



Title: ESD TESTS ON InP HEMT TRANSISTORS

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INTRODUCTION

The purpose of this report is to present the results of ESD tests performed on different HEMT transistors using a Human Body Model (HBM). The transistors tested were Mitsubishi (AsGa), TRW $200 \times 0.1 \mu\text{m}$ (InP), ETH $150 \times 0.2 \mu\text{m}$ (InP), and HRL $150 \times 0.1 \mu\text{m}$ (InP). The Human Body Model simulates the discharge of ESD from a human model. It is modeled by a 100pF capacitor discharged through a switching device and a 1500Ω series resistor into the device. Test fixtures specially built to measure the S-parameters of the transistors were used to apply the voltage to the transistor without protection circuit (see fig 1). The discharge was applied only at the gate of the transistor since this is considered to be the most sensitive part of it. The degradation was monitored by measuring the V_d/I_d curves of the transistor at ambient temperature.

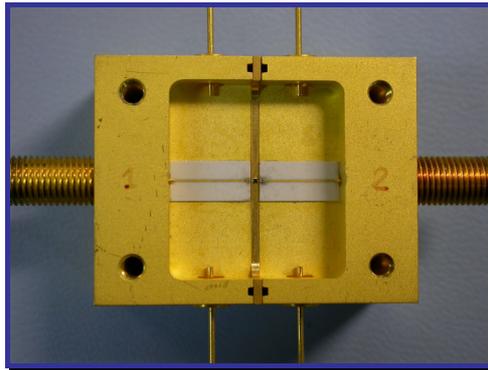


Figure 1.- Test fixture used in the measurements.

The lack of sensitivity levels defined by the manufacturer of the devices and the identification of such devices as Level 3 definition (HBM sensitivity $<20\text{V}$)¹ make us define a rejection level in the bias circuit of the amplifier that is considered safe for the device. The results obtained for the different devices are presented in this document together with the rejection needed to prevent damage in the transistors mounted in the IF1 amplifiers for HIFI ($TRW 200 \times 0.1 \mu\text{m}$ InP) due to Electrostatic Discharge.

Some devices can be severely damaged by ESD events of thousands of volts without being noticed by most people. In figure 2 a detail of the gate of one transistor possibly destroyed by ESD is shown. Note the metallization melt at the junction between the gate finger and the triangle connected to the gate bonding pad.

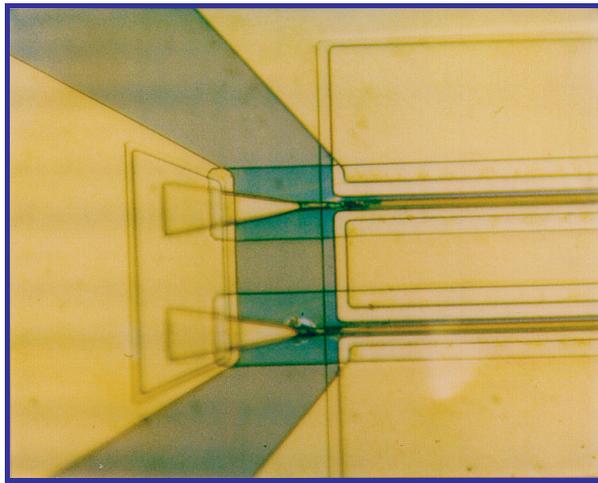


Figure 2.- Detail of an ETH $150 \times 0.2 \mu\text{m}$ InP HEMT transistor destroyed by ESD.

¹ As given in Document SRON-G/FPU/PL/2001-00x

DEVICES

The aim of the ESD tests carried out in our lab was the definition of the sensitivity of the devices used in the IF1 amplifiers for HIFI (TRW $200 \times 0.1 \mu\text{m}$ InP HEMT). However, it was decided to tests also other devices available in our institute and coming from different foundries. The devices tested using the HBM are shown in figures 3-6.

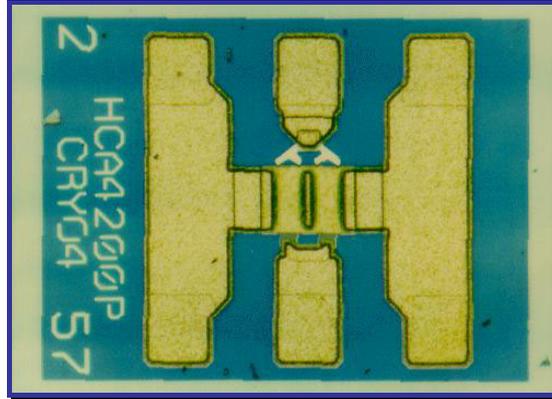


Figure 3.- TRW $200 \times 0.1 \mu\text{m}$ InP HEMT transistor used in the IF1 amplifiers for HIFI.

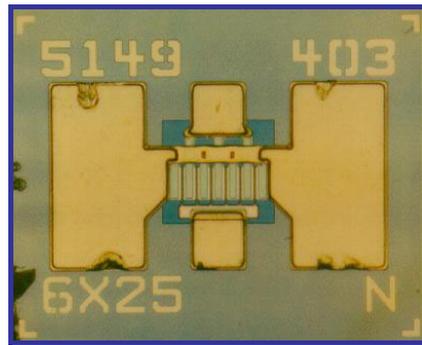


Figure 4.- HRL $150 \times 0.1 \mu\text{m}$ InP HEMT transistor.

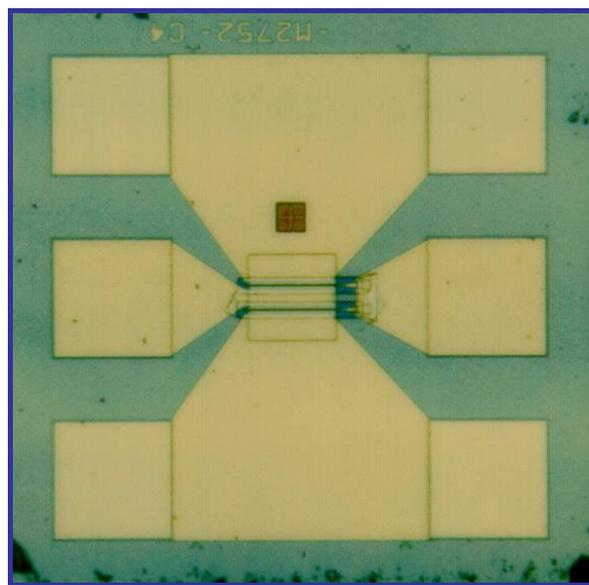


Figure 5.- ETH $150 \times 0.2 \mu\text{m}$ InP HEMT transistor.

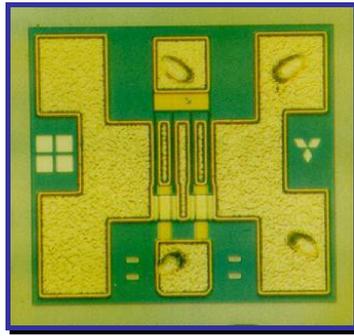


Figure 6.- Mitsubishi GaAs HEMT transistor.

HBM

The Human Body Model is a circuit representing the ESD from a human body and it is the model most commonly specified where people are handling ESD sensitive devices. The circuit used in our laboratory is shown in fig. 7.

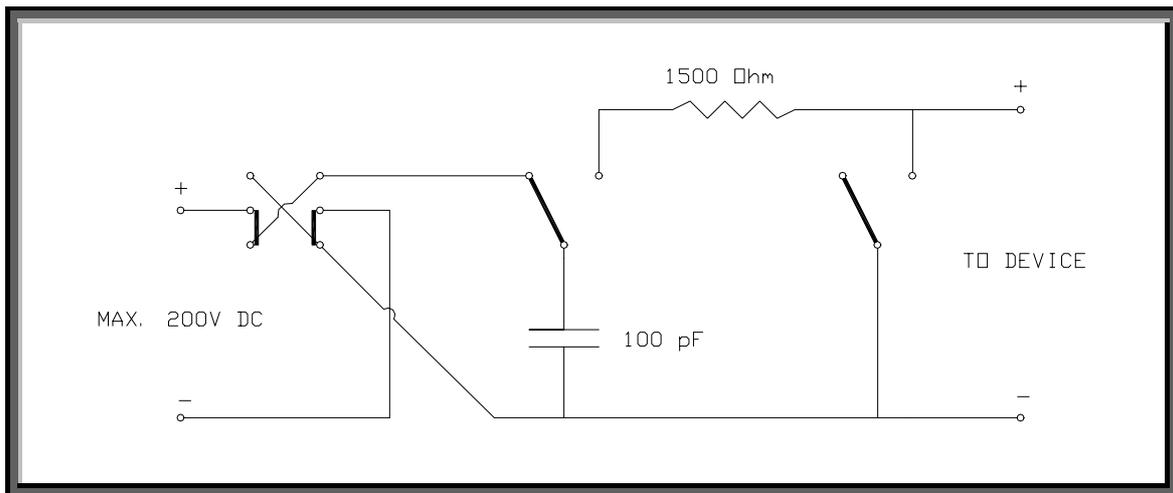


Figure 7.- Human Body Model representing the ESD from a human body.

RESULTS

The sensitivity levels for all the devices tested are presented in table 1. Figures 8 and 9 show the V_d/I_d characteristic for the TRW 200 μm InP HEMT transistor before and after an electrostatic discharge of 45V using the HBM.

Table 1.- Sensitivity level of the devices tested using the Human Body Model.

DEVICES	SENSITIVITY (V)
TRW 200 \times 0.1 μm InP HEMT	45
HRL 150 \times 0.1 μm InP HEMT.	80
ETH 150 \times 0.2 μm InP HEMT	100
Mitsubishi GaAs HEMT	200

It is important to note that only one transistor from each foundry was tested and the results got are not statistically significant. However, a rough indication of the sensitivity levels can be obtained. For the same reason, comparison of results of different devices should be done with caution.

As one would expect, the best devices (higher F_T , lower T_n) are the most sensitive to Electrostatic Discharges.

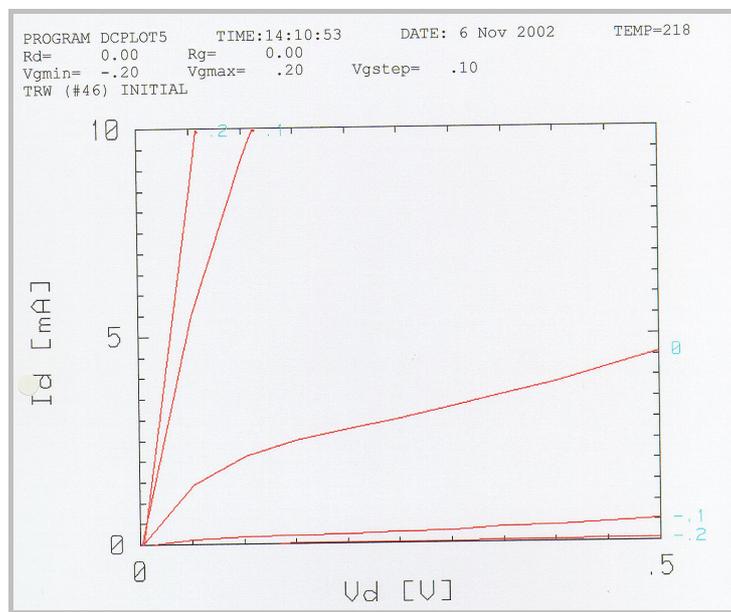


Figure 8.- TRW 200 μm InP HEMT V_d/I_d characteristic before an electrostatic discharge.

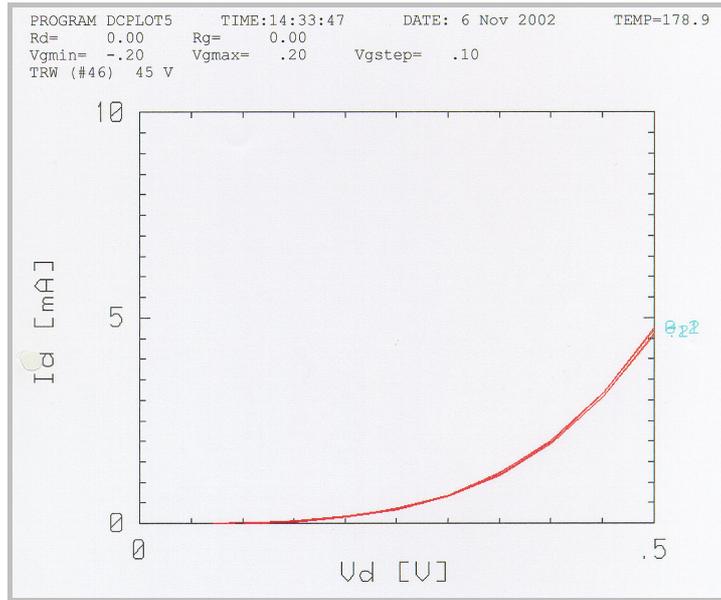


Figure 9.- TRW 200µm InP HEMT V_d/I_d characteristic after an electrostatic discharge of 45V.

PROTECTION CIRCUIT

The results presented were got applying the electrostatic discharge directly to the transistor without a protection circuit. However, in a real amplifier for HIFI, a protection circuit to prevent damage in the gate of the transistor is implemented (fig. 10). In this section we will try to find out the ESD sensitivity level of the assembled amplifier.

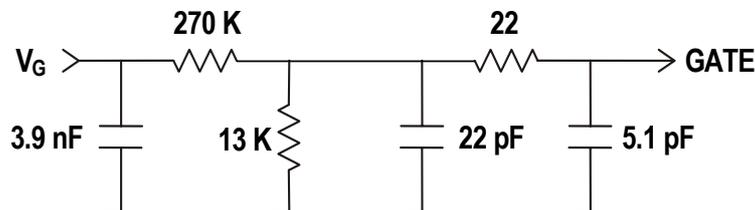


Figure 10.- Protection circuit at the gate of the transistor in a HIFI amplifier.

The protection circuit is composed of the 3.9nF capacitor and a resistive voltage divider. There is a ratio of 40 due to the charge division between the 100pF of the HBM and the 3.9nF at the input of the protection circuit. An additional ratio of 21 is due to the voltage divider. All this combined give us a factor of 840 of protection what means that considering a sensitivity level of 45V at the transistor side, the damage level at the bias connector will be 37.800V.

CONCLUSIONS

ESD tests on different HEMT transistors using a Human Body Model (HBM) have been performed and the protection of the bias circuit of a assembled amplifier using TRW 200x0.1µm InP HEMT devices has been estimated. The ESD sensitivity level of the TRW device tested was 45V. This indicates that the devices can be classified as level 2 (HBM sensitivity <100V)¹ instead of 3. The protection circuit in Figure adds a factor of 840, giving a theoretical ESD sensitivity level of 37.800V at the DC connector. This means that the assembled unit can be classified as level 0 (HBM sensitivity >1000V)¹. However, the estimated level at the DC connector has not been measured in practice and should be taken with caution.