Title: MEASUREMENTS OF BIAS FILTERS OF IF1 AMPLIFIERS MODEL YCF SERIES 6000

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INTRODUCTION

The purpose of this report is to present the results of the tests performed on test fixtures specially built to study the properties of the bias circuit of the IF1 cryogenic amplifier of the Focal Plane Unit of HIFI instrument. The rejection in the range from 10 MHz to 10 GHz has been measured, and the results are compared with the theoretical model of the circuit, including first order parasitic in the components. The aim is to gain understanding on the limitations and the validity range of the models used for the bias components and to improve the knowledge of the performance regarding EMC.

In a second part, some measurements of transmission through the bias lines of a complete working amplifier were taken. The signal was injected in each line of the bias connector of the amplifier (biased and unbiased) and the power detected at the output was measured. This is not a very accurate measurement due to the length of unshielded cable used at the bias connector side, but it gives a rough estimation of the efficiency of the bias filtering. The results obtained are compared with the EMC measurements.

BIAS FILTERS

- **MODELS**

Figures 1 and 2 show the circuit used for the simulation of the bias network. The first order parasitics of the elements are included. The values of the parasitics are based on measurements of the components. The 10 nF capacitor and the 27 Ohm and 270 K resistors were measured in a Vector Network Analyzer. The models of other components (ATC capacitors of 22 and 5.1 pF and the 22 Ohm State of the Art resistor) were previously known, as they are used for the design of the RF part of the amplifier. The inductance of the bonding wires was included when applicable. Other effects, like electrical length or impedance of interconnecting lines, are not considered.

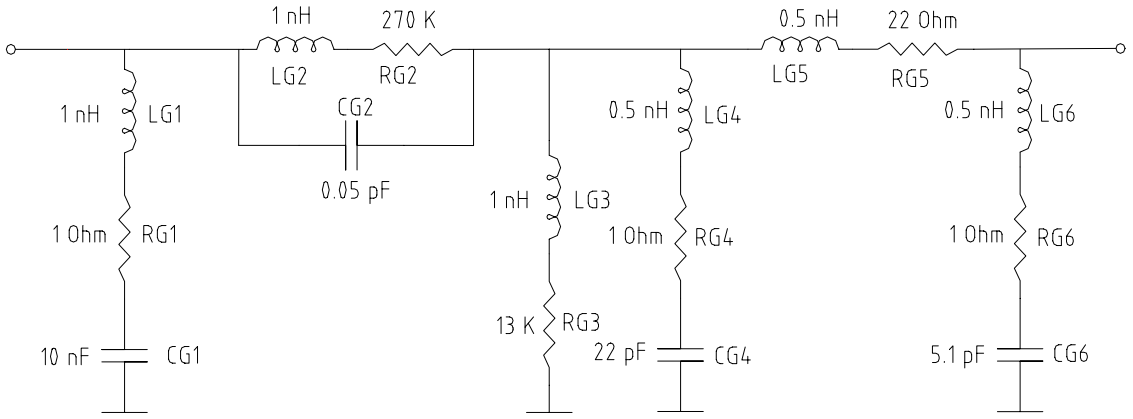


Figure 1: Model of gate bias network including parisitics. CG1, RG2, RG3, CG4, RG5 and CG6 are the main elements. The rest are the parasitics considered. Left side is connected to DC input and right side to the gate of the transistor. The circuits of the first and second stages of the amplifier are identical.

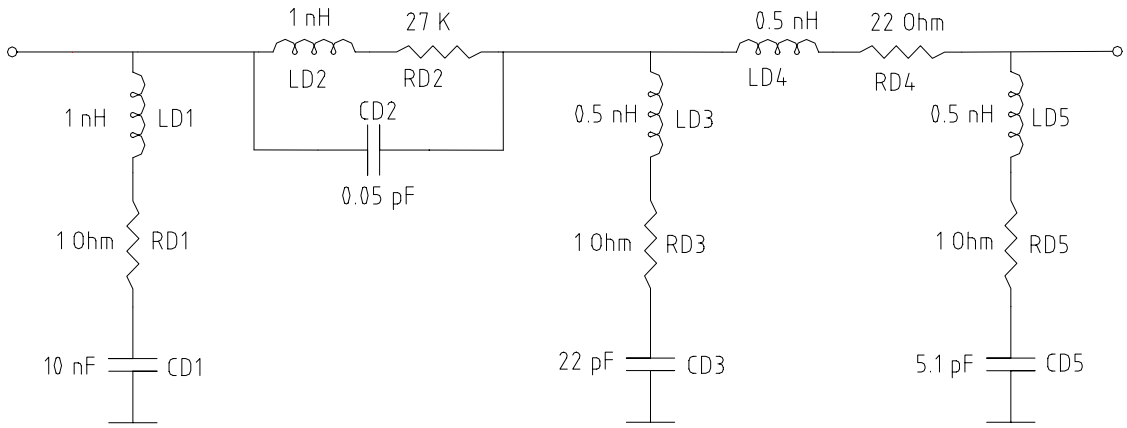


Figure 2: Model of gate bias network including parisitics. CD1, RD2, CD3, RD4, and CD5 are the main elements. The rest are the parasitics considered. Left side is connected to DC input and right side to the drain of the transistor. The circuits of the first and second stages of the amplifier are identical.

- **PHOTOS**

Figure 3 shows the drain bias circuit used in the measurements. It was mounted on a standard fiberglass printed circuit board with continuos ground plane on the backside. The SMD components are of the same type and size used in the bias circuit of the amplifier. The ground connection of the 10 nF capacitor was done with via holes. The microwave components (ATC capacitors of 22 and 5.1 pF and SOA resistor of 22 Ohms) were mounted in a hole milled in the board, in order to reproduce the technique used in the amplifier. The layout of the circuit, the board material and the properties of the enclosure differ from those of the final amplifier, but as the components used and the mounting techniques are identical it is expected to obtain a reasonable representation of the filter.

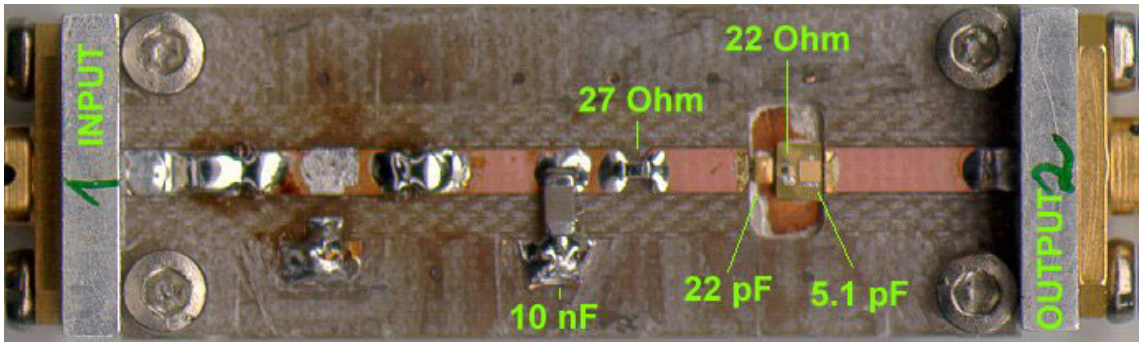


Figure 3: Board used for the measurements of the drain bias circuit.

• RESULTS

The results obtained in the measurement, compared with the prediction of the simple model used are presented in figure 4. For the drain bias filter the agreement between the measurements and the model is good in general, with the exception of the ripple appearing between 3 and 5 GHz. The gate bias filter shows worst agreement, due in part to a poorer construction of the circuit board. The goal of obtaining a rejection better than 30 dB (20 dB minimum)[1] in the frequency range from 10 MHz to 4 GHz is accomplished clearly with the present configuration of the gate bias filter, and marginally with the drain circuit.

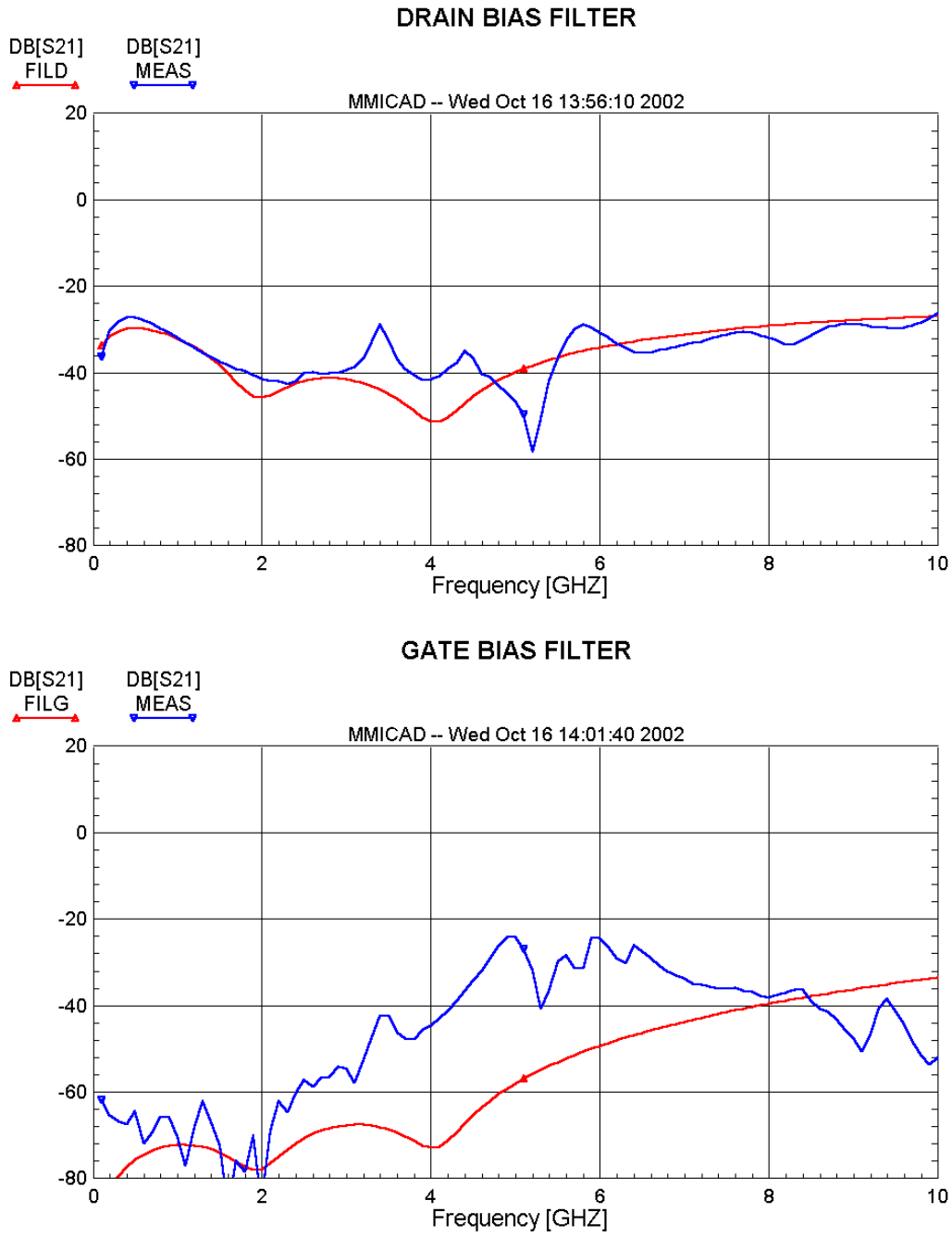


Figure 4: Comparison of measurements and model of the drain and gate bias filters.

[1] As agreed in IF-1 progress meeting of 28/05/02, doc. number SRON-G/HIFI/MM/2002-001

- **IMPROVEMENTS**

As it has been shown in previous section, the drain bias filter should be improved. A ferrite bead connected at the input and a piece of ferrite absorber covering the input line were tested, but the effect at the low frequency end was very little. The most efficient way found to improve the rejection in the 10 MHz to 4 GHz region was to add a series 27 Ohm resistor and a 10 nF capacitor to ground at the input (left) side of figure 2. Figure 5 presents the measured and modeled data of this configuration. Figure 6 shows the improvement obtained respect to the original configuration. The new resistor may add an additional 0.25mW of power dissipated in each stage of the amplifier (a total of 0.5 mW per amplifier).

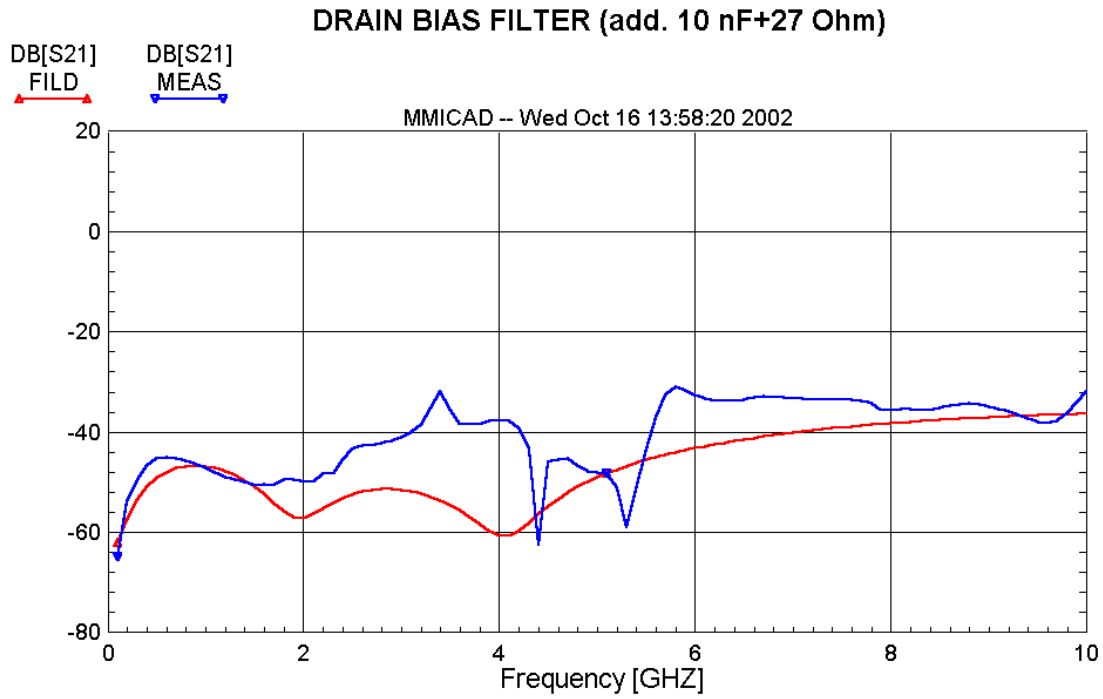


Figure 5: Transmission of the drain bias filter with an additional 10 nF capacitor and 27 Ohm resistor on the input side.

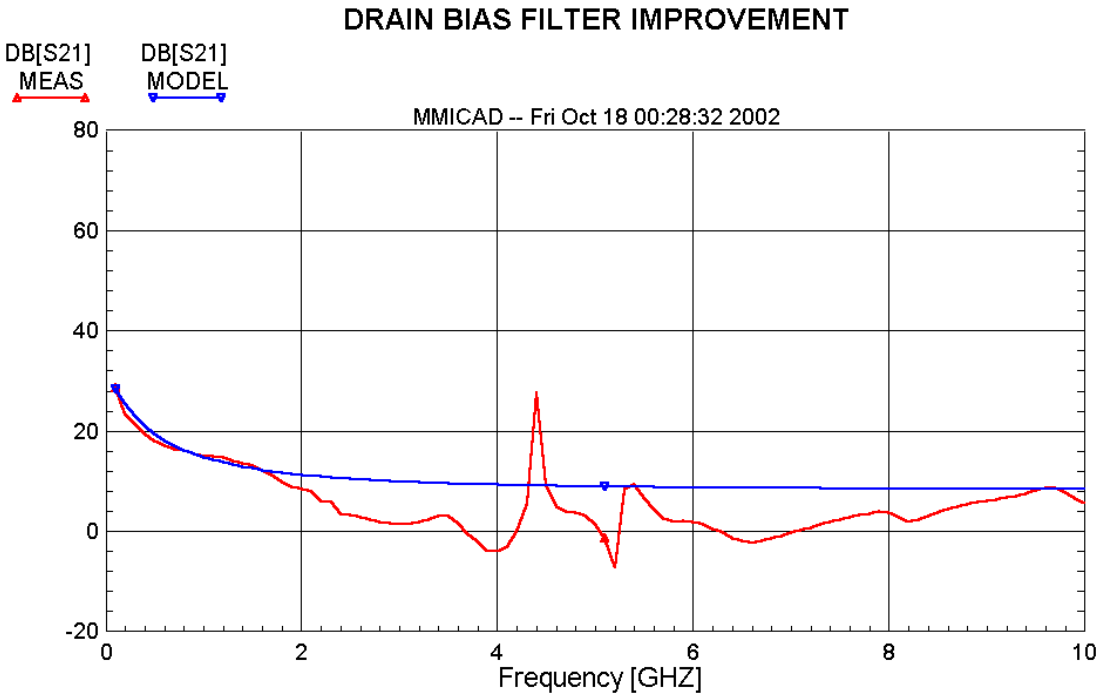


Figure 6: Improvement in the transmission of the drain bias filter with an additional 10 nF capacitor and 27 Ohm resistor on the input side.

BIAS FILTERING MEASUREMENTS OF YCF 6001 AND AEO01 AMPLIFIERS

Two amplifiers of the DM type were tested for bias filtering. One of the amplifiers was built in Yebes and the other in Alcatel. They differ only in the layout of the bias circuit. In the amplifier made in Yebes the inductance to ground of the 10 nF capacitors is expected to be greater, since the connection is made with bonding wires. The amplifier made in Alcatel makes use of plated trough holes for the same function. Figure 7 shows a picture of the setup used in the measurements. The signal is injected on each of the bias lines (one at the time). The DC power for bias is introduced in the line tested using the bias tee of the VNA. The input of the amplifier is terminated in a matched load. Figures 8 and 9 present the results of the measurements with bias on and off. Each graph presents four plots, one for each of the bias lines. In contradiction to the expectations, and for unknown reasons, the results at the low frequency end are slightly better for the amplifier made in Yebes. Figure 10 shows the predictions of the model for the measurements made. Figure 12 is a representation of the same data as in figure 8, but in a form easily comparable with measurements of EMC. In an EMC measurement the device is tested under a constant field. The power level injected in the bias cables depends on the "gain" of the cables acting as an antenna picking up the radiated field. In general the antenna factor of the bias cables will show very complicated frequency dependence. For a rough estimation, the transmission graph is transformed assuming a simple dependence of the antenna gain of the form $1/f^2$.

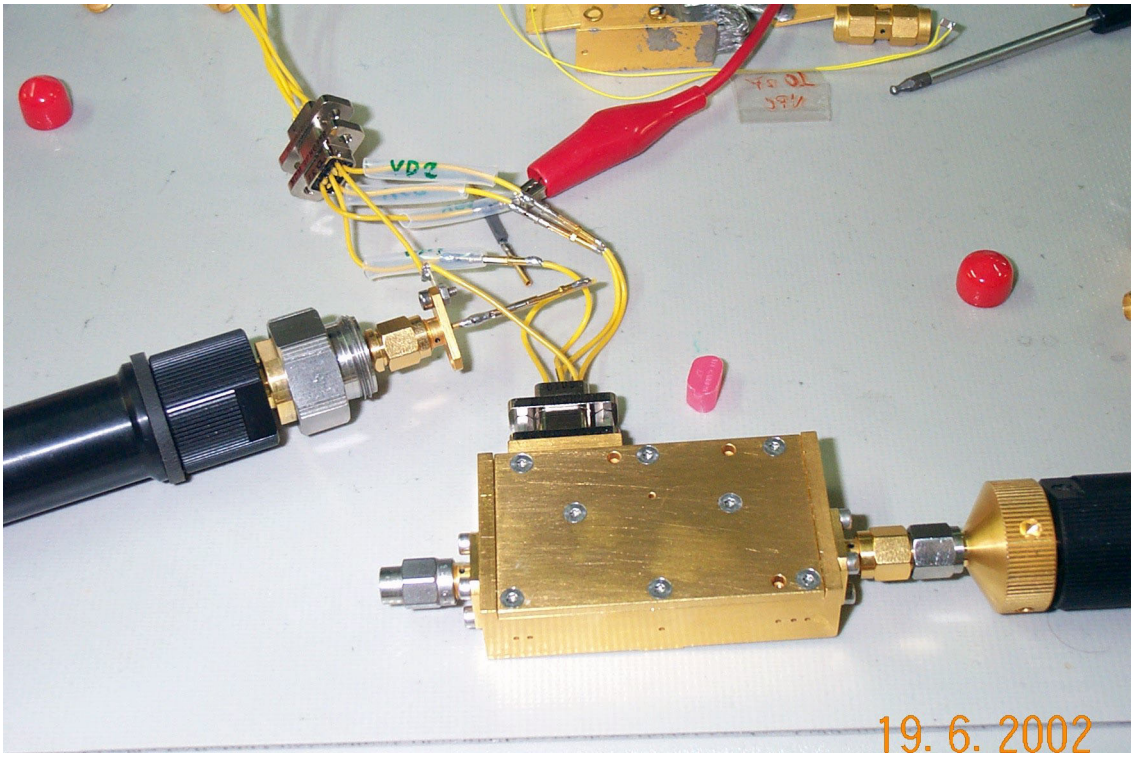
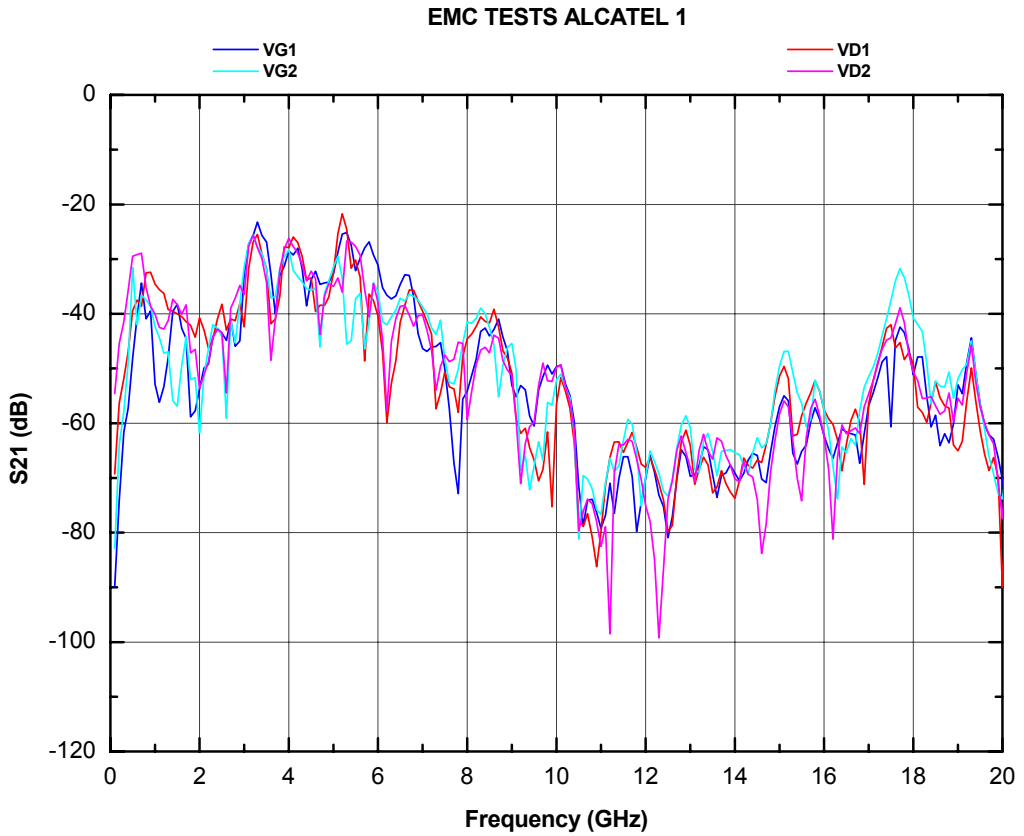


Figure 7: Measurements of the bias filter of the amplifier with the Vector Network Analyzer.



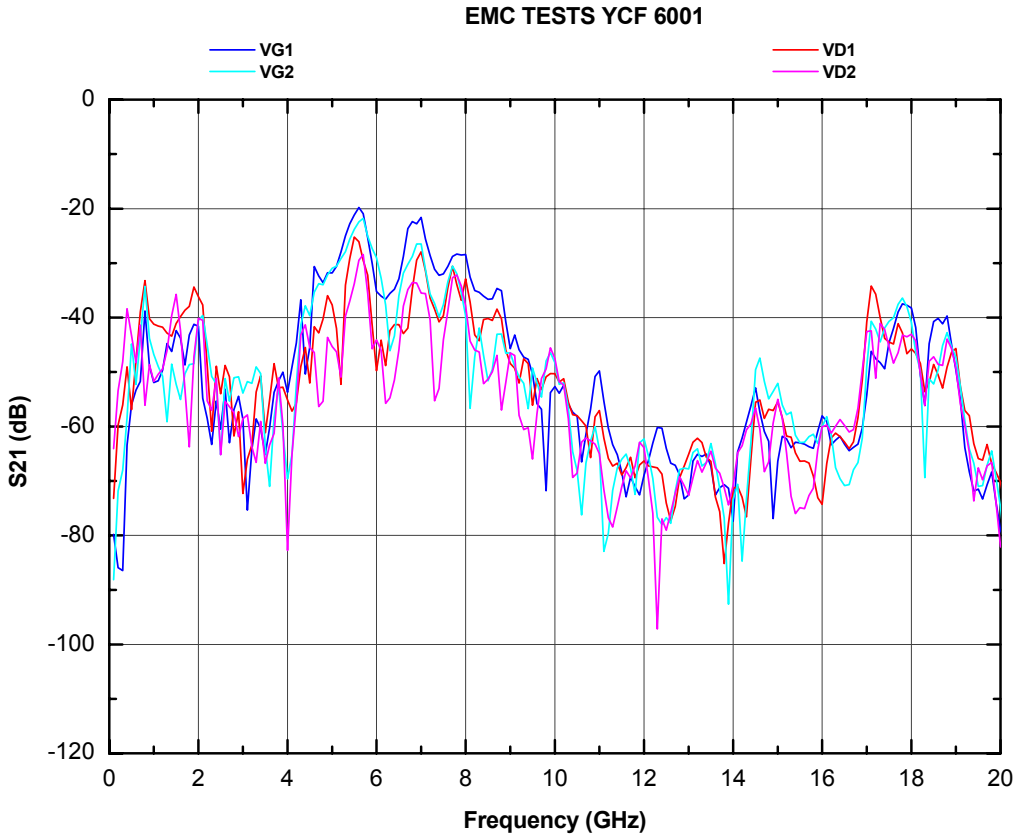
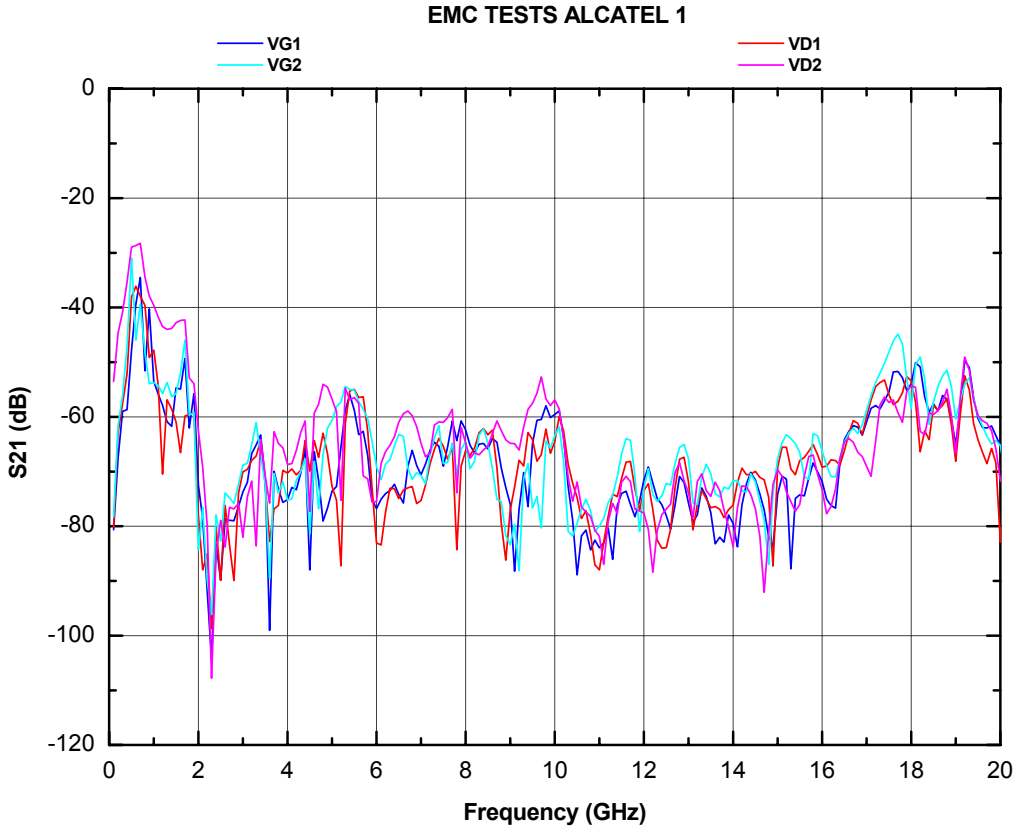


Figure 8: Tests of bias filter of Alcatel and Yebes amplifier (Bias ON).



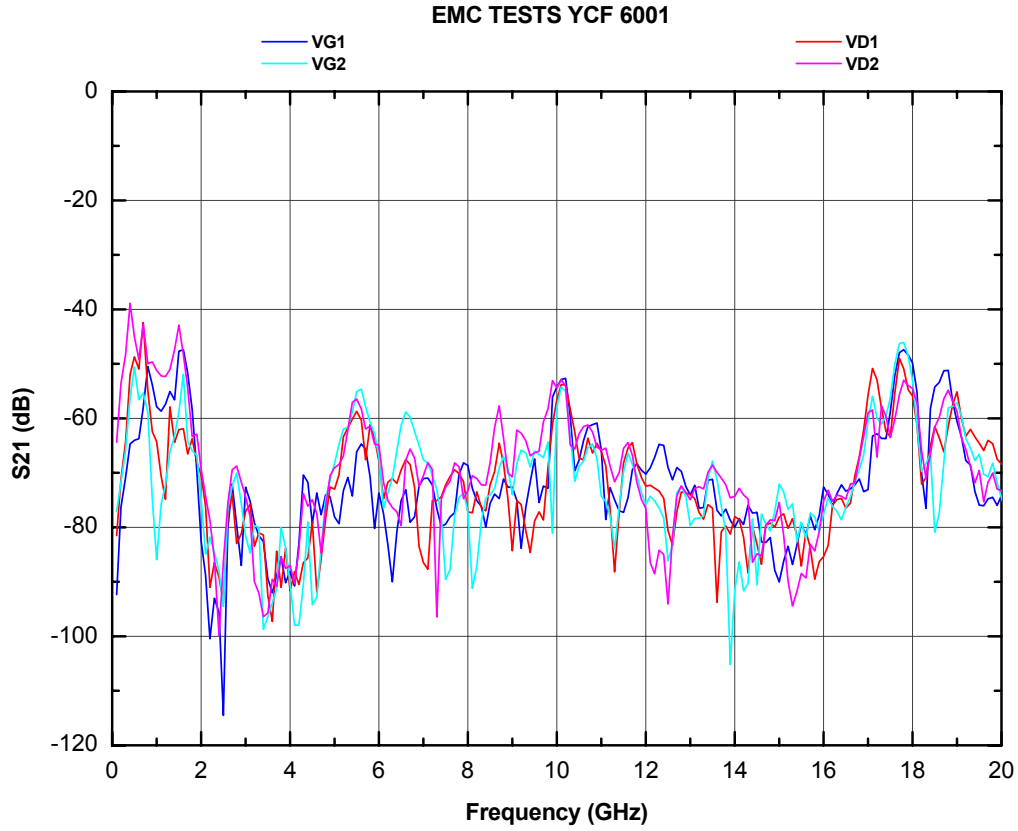


Figure 9: Tests of bias filter of Alcatel and Yebes amplifier (Bias OFF).

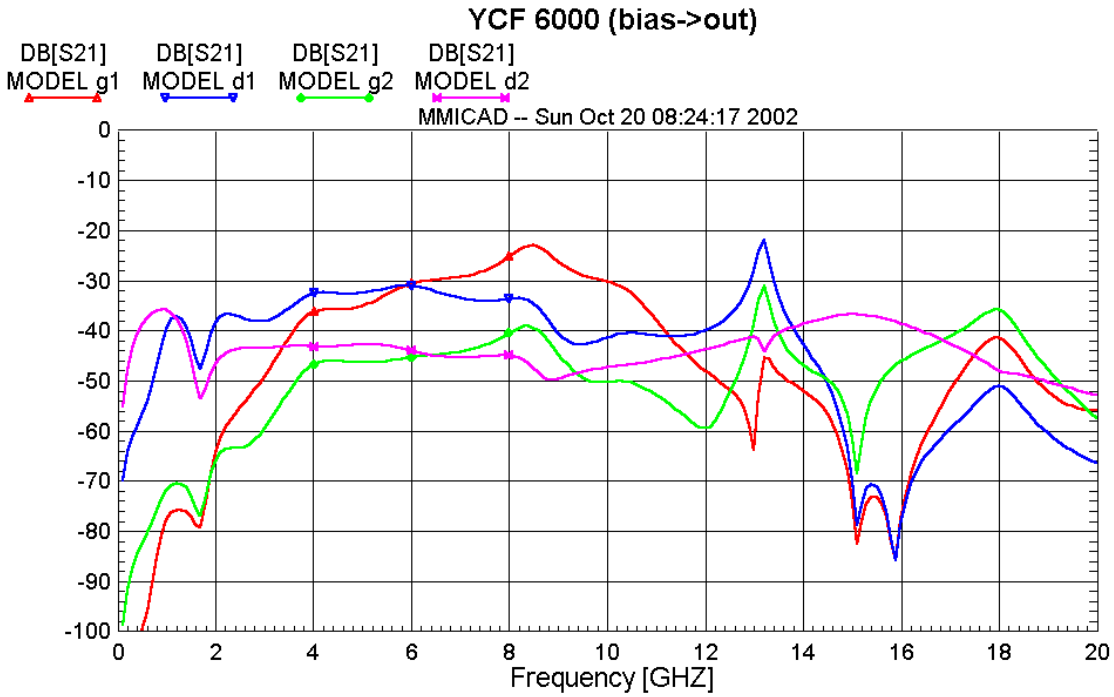
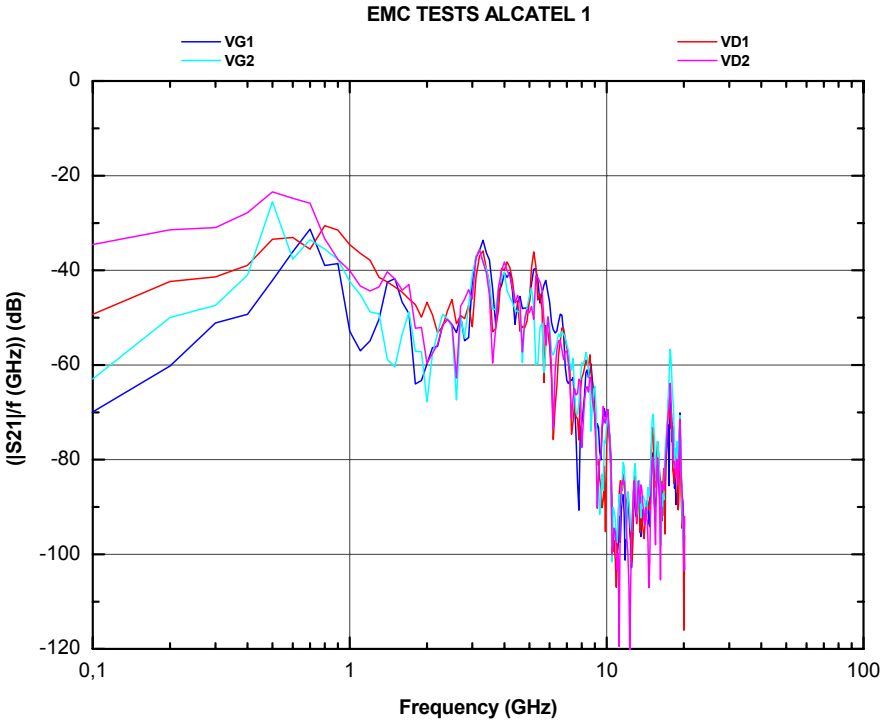


Figure 10: Model of the bias filter effect in the amplifier (Bias ON).



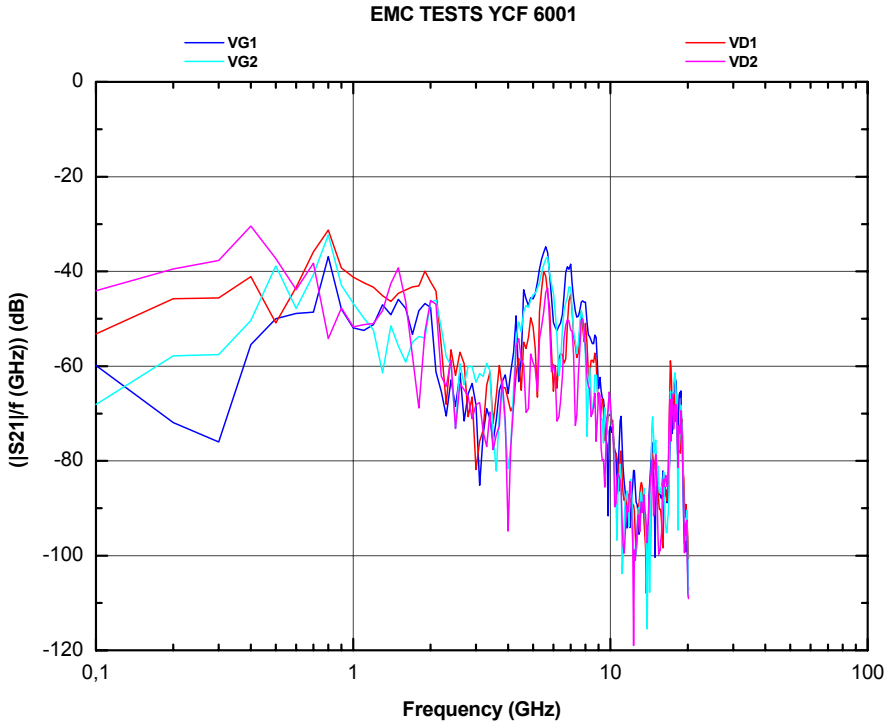


Figure 11: Test of transmission from bias to output in Alcatel and Yebes amplifier. Data is the same as in figure 9, but now in the vertical axis the variable presented is S21 divided by frequency in GHz. This plot is intended for comparison with the measured EMC data, since it is corrected for the rough dependence of the antenna factor.

CONCLUSION

From the measurements of the bias filters it was clear that the rejection could be improved by adding a 10 nF capacitor to ground and a series 27 Ohm resistor in the input side. This will have an impact in the power dissipation of the amplifier. The power will be increased to approximately 0.5 mW in a two-stage amplifier[2]. Other methods tested (ferrite beads at the input or pieces of ferrite absorber) do not allow improving the rejection at low frequencies as easily as the RC filter.

The measurements of transmission from the bias lines to the output show reasonable levels, but do not follow the pattern expected from model calculations. Besides, the small change in the configuration of the bias circuits in the two amplifiers tested (one made in Yebes and the other in Alcatel) has an important impact in the measured performance. The measured transmission is quite similar for any of the four DC input lines. As this is not what was predicted by the model, it is possible that the coupling of the bias lines inside the amplifier may play an important role in the measured performance.

The measured EMC performance[3] showed some peaks in the low frequency region (below 1 GHz). These peaks do appear in the present transmission measurements. The improvement in the rejection of the drain bias filters in this frequency region should help in the reduction of these peaks.

Taking into account these results, and the requirement of having a second order loop in the gate bias lines for common mode rejection[4] we propose for the QMs and FMs the circuits appearing in figure 12. The gate bias filter is not identical to the one required[4] because of the limitations in the components available from the CPPA already defined, and because the practical limit to the maximum capacitance available for the cryogenic use (3.9 nF). The voltage division ratio is 21, very close to the previously agreed value. The input impedance changes from the old value of 270 K to 200 K. This will have a small impact in the power dissipated in the gate bias circuits (negligible compared with the power dissipated in the active amplifier). It is not expected to have problems related to this fact.

The model prediction of the new version of the filters is presented in figure 13.

[2] This increase in the power dissipation is within the limits of additional power asked to the consortium. The increase in power allowed is of 1 mW per amplifier. It will be safe to keep the margin as it is (1 mW) because it may be needed in case of variations in the performance of the batch of, or for the need of additional resistance in the bias filters in a later analysis.

[3] Bert-Joost van Leewen, "Radiated E-field susceptibility of varios FPU components," HIFI report no. SRON-U/FPU/RP/2002-001.

[4] CM analysis of IF amplifier bias supply interface (IF-1 progress meeting of 28/05/02, doc. number SRON-G/HIFI/MM/2002-001).

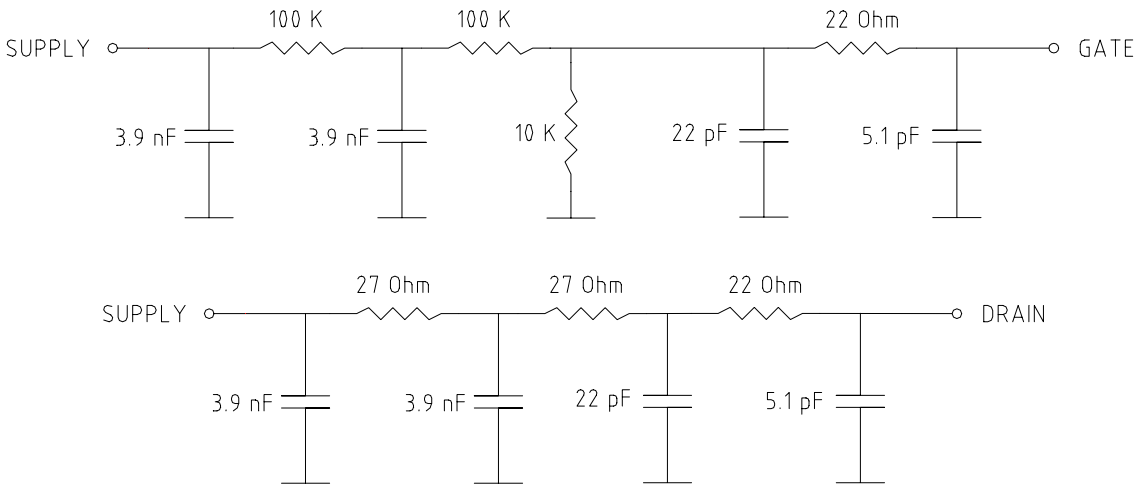


Figure 12: Proposed bias filter circuits for FMs.

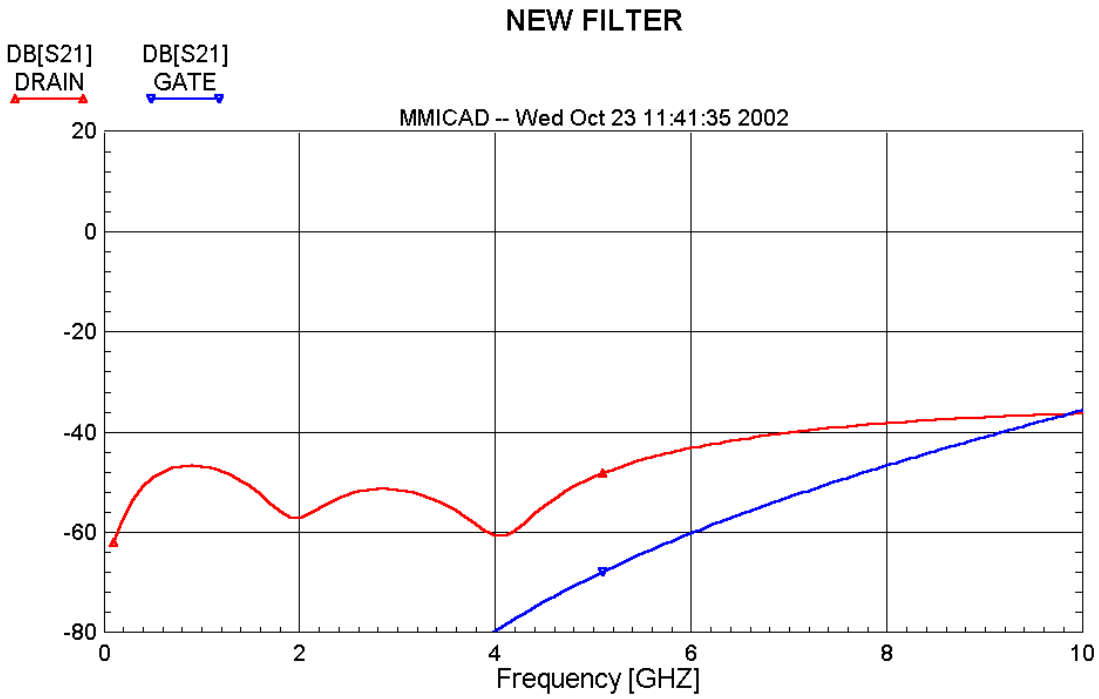


Figure 13: Transmission for the new bias filters proposed as calculated in the model.