Centro Astronómico de Yebes

CAY

CRYOGENIC AMPLIFIER REPORT

YCA 2011 0703

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2. HEMT bias card report
3. ESD and power supply leakage protection of InP cryogenic HEMT amplifiers

YCA 2 4-8 GHz AMPLIFIER REPORT

1. Introduction

YCA series 2 are C band, 4-8 GHz low noise cryogenic amplifiers designed and built at the *Centro Astronómico de Yebes* for the development phase of the ALMA project. They will be used as first stage IF amplifiers. This document includes a description of the amplifiers and how to operate them, details about the tests performed, the measurements techniques utilized, plots and tables with the relevant data collected (an index is provided thereafter) and a summary page introducing the measurements.

The amplifier is intended to be used together with a **cryogenic isolator** connected to its input. PAMTECH has designed several 4-8 GHz models for this purpose like the CTH1365K4 and the CTH1365K10.

The unit should be biased by a **servo controlled power supply**, which sets the gate voltage for any given drain current. Details about a NRAO style power supply produced in Yebes for our HEMT amplifiers are given in the "HEMT bias card report" section.

2. Description and operating conditions of the amplifier

- Figure 1 shows an outside view of the amplifier. RF input and output connectors are SMA. DC connector is a 9 pin microminiature D-type ITT-Cannon. The pinout is provided in figure 2. As seen in the figure, the RF input connector is the one located closer to the DC connector; the serial number of the unit is stamped on the long side of the amplifier, besides de DC connector. All the holes used to fix the lid are M2 thru-holes and can be used from the other side to attach the amplifier to a cold plate. Be aware of the limited length of thread available, due to the small height of the amplifier.

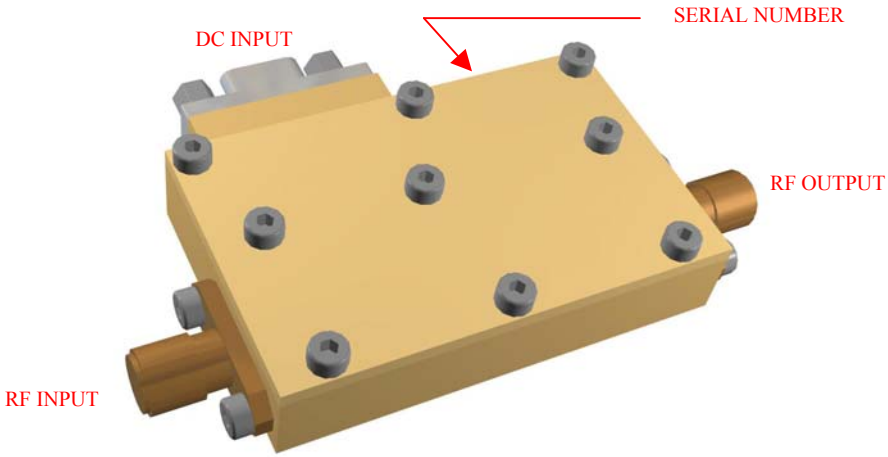
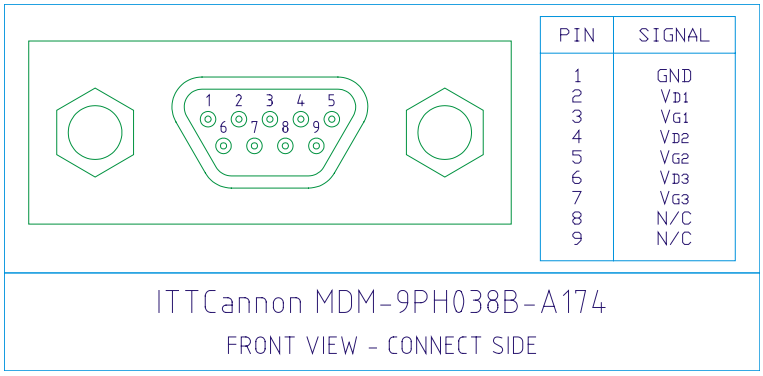


Figure 1: *YCA 2 amplifier external elements*

- The external dimensions and mechanical interfaces of the amplifier are shown in figure 4.
- YCA 2 are three stage amplifiers implementing TRW [1] and ETH [2] InP transistors. The InP devices are very **ESD sensitive**; cautions must be taken in its manipulation. The bias circuits built in the amplifier include a 10 nF capacitor which acts as a charge divider to prevent damage to the transistors, but no diodes. A ~1:10 voltage divider is also implemented at the gates input lines to improve EMC and protect against ESD: high operating values of the gate voltages are normal. A schematic of these circuits is shown in figure 3. Information on ESD prevention procedures, and safe unit handling and storage is provided in the "ESD and power supply leakage protection of InP HEMT cryogenic amplifiers" section.
- One bias condition has been selected for the amplifier, which optimizes the device for noise, gain ripple, output reflection and gain fluctuations, *keeping the power dissipation below **9 mW***. Some improvement in noise and gain may be expected using a higher bias. Never exceed a drain voltage/current of 1.5 V / 10 mA for InP transistors.



PIN	SIGNAL
1	GND
2	VD1
3	VG1
4	VD2
5	VG2
6	VD3
7	VG3
8	N/C
9	N/C

Figure 2: *DC Connector pinout*

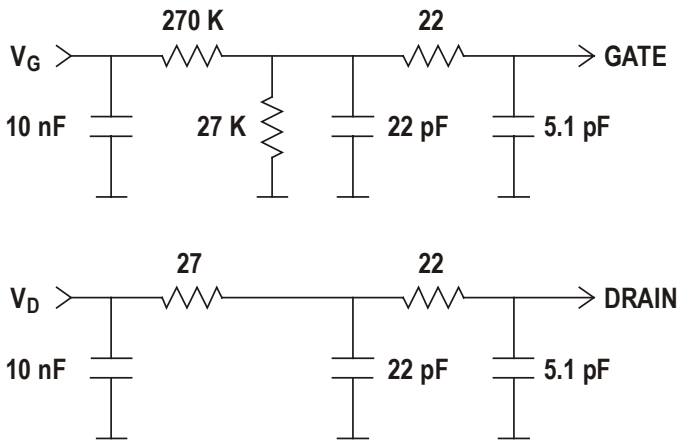


Figure 3: *YCF 6 bias circuits (inside the amplifier)*

[1] Transistors provided by TRW under contract with JPL, as part of the NASA Cryogenic HEMT Optimization Program (CHOP).
[2] Transistors provided by ETH under contract with IRAM.

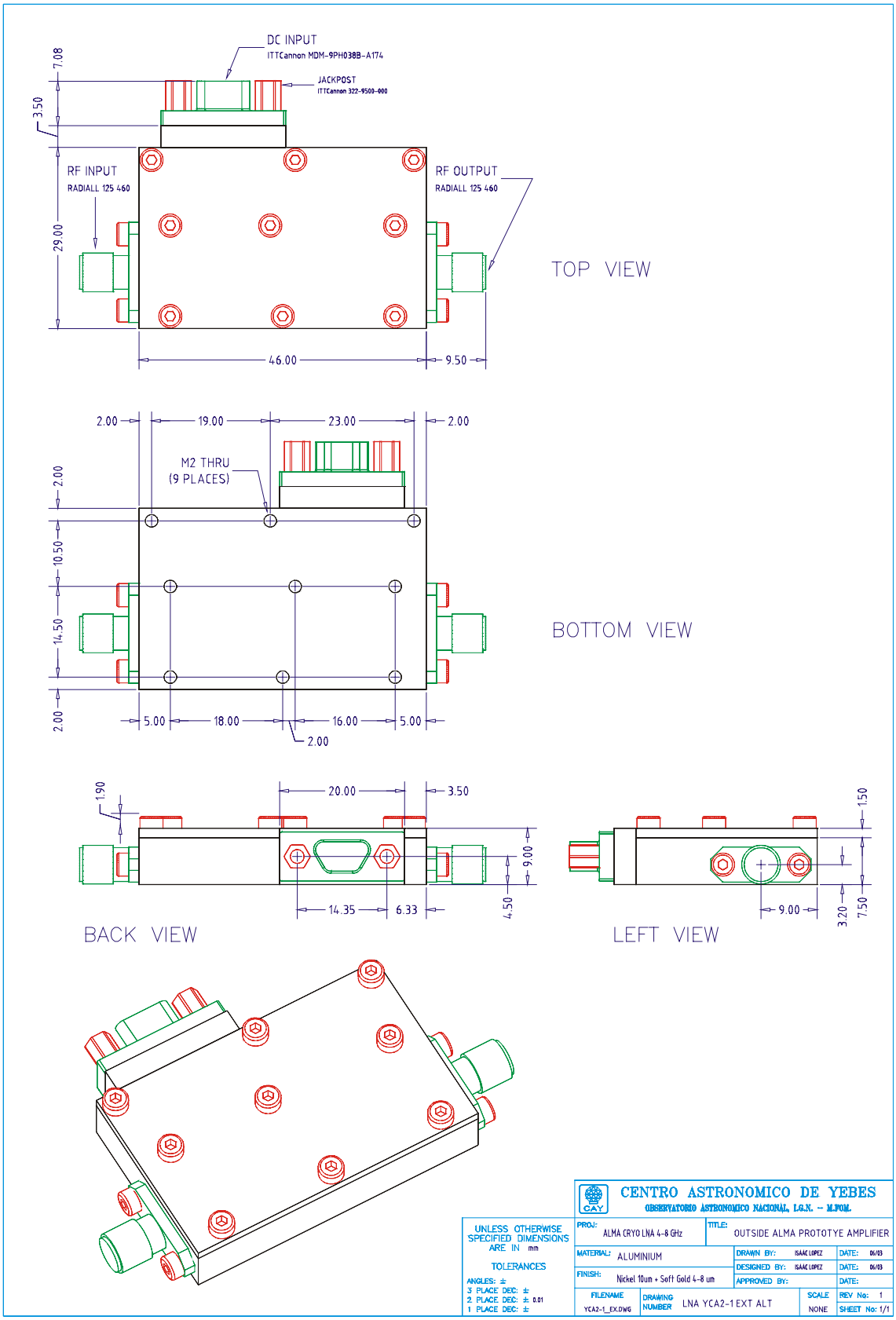


Figure 4: *YCA 2 external dimensions*

3. Measurements

3.1 Description

Noise temperature (and gain) was measured with a system based in a computer controlled HP 8970 B Noise Figure Meter described in detail in [1]. Room temperature data was obtained with an HP 346 A noise diode. The DUT is cooled in a dewar with a CTI 350 refrigerator. Cryogenic measurements were taken with the "cold attenuator" method, using an HP 346 C noise diode (at room temperature) plus a 15 dB attenuator and a DC-Block cooled at cryogenic temperature (the DC-Block is included to avoid heating the active part of the attenuator by the inner conductor of the stainless steel coaxial line). Temperature is carefully monitored in the attenuator body using a Lake Shore sensor diode. The accuracy of the system for the amplifiers measured can be estimated with methods presented in [1], [2]. For present case, absolute accuracy (@ 3 σ) of measured noise temperature is estimated in ±9 K at T_{amb}=297 K and ±1 K at T_{amb}=14 K. Repeatability is better than this values by an order of magnitude.

Reflection and gain of the unit in the 350 dewar, at room and cryogenic temperatures, were measured using an HP 8757 A Scalar Network Analyzer in AC (modulated) mode. Note that the amplifier design is not optimized for input reflection, as it is intended to be used with an isolator at the input.

The same system, but in DC (non-modulated) mode was used to detect possible oscillations. The amplifier was tested at room and cryogenic temperature with one sliding short connected to the input and another to the output, and the wide band detector connected to the output. The test was repeated with an Agilent 9565 EC spectrum analyzer. No oscillation was detected in the normal bias range. With very high voltages in the first and second stages, some amplifiers oscillate around 33 GHz. Further increasing these voltages another oscillation appears around 8 GHz.

S parameters of the amplifiers were measured with the HP 8510 C Vector Network Analyzer from 0.1 to 20 GHz to compare with less accurate SNA measurements, and to check for signs of possible out of band instability. This test was done at room and cryogenic temperature for selected amplifiers, showing no sign of instability (Rollet constant greater than 1 at all frequencies), and good agreement with SNA data.

Gain stability (short term) was measured in a dewar with a CTI 1020 refrigerator, at a single frequency (6 GHz) using a continuously variable attenuator, air lines and the HP 8510 C Vector Network Analyzer, according to [3]. The results are presented in form of spectral density of normalized gain fluctuations. Several spectrums, in the range 0.012-2.34 Hz, are obtained by FFT of the VNA time domain data and averaged to reduce random fluctuations. The plots also show the value of the contribution of the system fluctuations, which is subtracted from the measurements. The reference value of the fluctuations at 1 Hz (β) is also given, and its units are $1/\sqrt{Hz}$ (when the exponent α is 0.5). There is usually a peak at 1 Hz due to the cycle of the CTI 1020 refrigerator. In the same page phase fluctuation data are also are provided in a similar fashion.

3.2 Index of plots

We provide plots of the scalar analyzer measurements, noise figure meter measurements and Mathcad files from vector analyzer measurements at ambient and cryogenic temperatures, for the optimum bias point.

1. Summary of performance, characteristics and bias
2. Cryogenic measurements
    a. Noise temperature & gain
    b. Input reflection loss & gain (up) and output reflection loss (down)
    c. Gain stability
3. Room temperature measurements
    a. Noise temperature & gain
    b. Input reflection loss & gain (up) and output reflection loss (down)
    c. Gain stability

References

[1] J. D. Gallego, "*Amplificadores Refrigerados de muy bajo ruido con transistores GaAs FET para la frecuencia intermedia de receptores de radioastronomía*," Tesis Doctoral, Facultad de Ciencias Físicas, Universidad Computense de Madrid, 1992.

[2] J. D. Gallego, M. W. Pospieszalski, *"Accuracy of Noise Temperature Measurement of Cryogenic Amplifiers*," Electronics Division Internal Report No. 285, National Radio Astronomy Observatory, Charlottesville, Virginia, March 1990.

[3] J. D. Gallego, I. López Fernández, *"Measurements of Gain Fluctuations in GaAs and InP Cryogenic HEMT Amplifiers*," Technical Report CAY 2000-1, February 2000.

CENTRO ASTRONÓMICO DE YEBES

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C-BAND CRYOGENIC AMPLIFIER REPORT

DATE: 3 sep 2003

BAND:	4 - 8	S/N:	*YCF 2011 0703*
TRANSISTOR 1st STAGE:	TRW 200x0.1 um T-52 (CRYO4)		
TRANSISTOR 2nd STAGE:	ETH 150x0.2 um T-51 (IRAM R3)		
TRANSISTOR 3rd STAGE:	ETH 150x0.2 um T-51 (IRAM R3)		

ROOM TEMPERATURE DATA (T=297 K)

OPTIMUM BIAS	V_{d1} =	1.25	I_{d1} =	10	V_{g1} =	0.23
	V_{d2} =	1.25	I_{d2} =	10	V_{g2} =	0.40
	V_{d3} =	1.25	I_{d3} =	10	V_{g3} =	0.40

AVERAGE NOISE TEMPERATURE:	65.5	AVERAGE GAIN ± RIPPLE:	37.7±1.2
MIN. OUTPUT RETURN LOSS:	12.0	GAIN FLUCTUATIONS @1 HZ:	4.00E-5

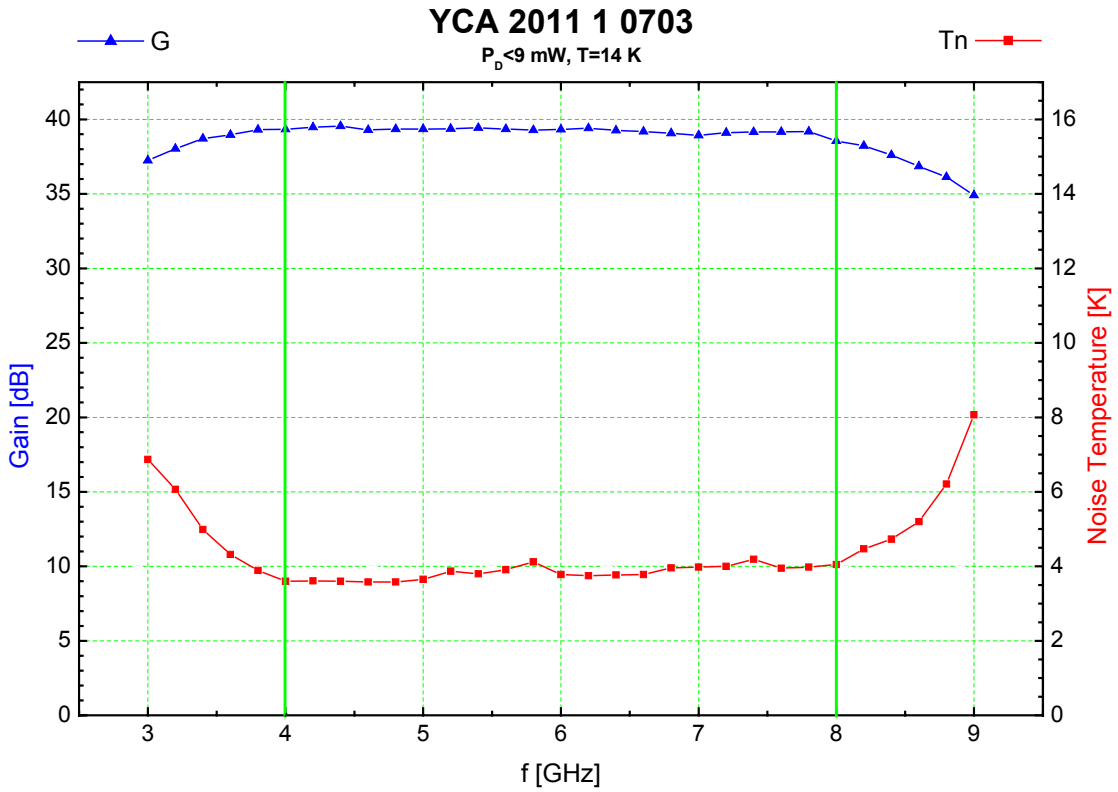
CRYOGENIC TEMPERATURE DATA (T=15 K)

OPTIMUM BIAS (9 mW)	V_{d1} =	0.7	I_{d1} =	4	V_{g1} =	1.36
	V_{d2} =	0.5	I_{d2} =	3	V_{g2} =	0.71
	V_{d3} =	1.2	I_{d3} =	4	V_{g3} =	0.44

AVERAGE NOISE TEMPERATURE:	3.8	AVERAGE GAIN ± RIPPLE:	39.0±0.50
MIN. OUTPUT RETURN LOSS:	13.0	GAIN FLUCTUATIONS @1 HZ:	7.21 E-5

REMARKS:

V_d in Volts, I_d in mA, Noise temperature in K, Gain and Return loss in dB, Frequency band in GHz, Gain fluctuations in 1/√Hz



NOISE AND GAIN MEASUREMENT PROGRAM WNOISE (350)

TIME 11:48:22 DATE : 15 Jul 2003 Tamb= 14.69

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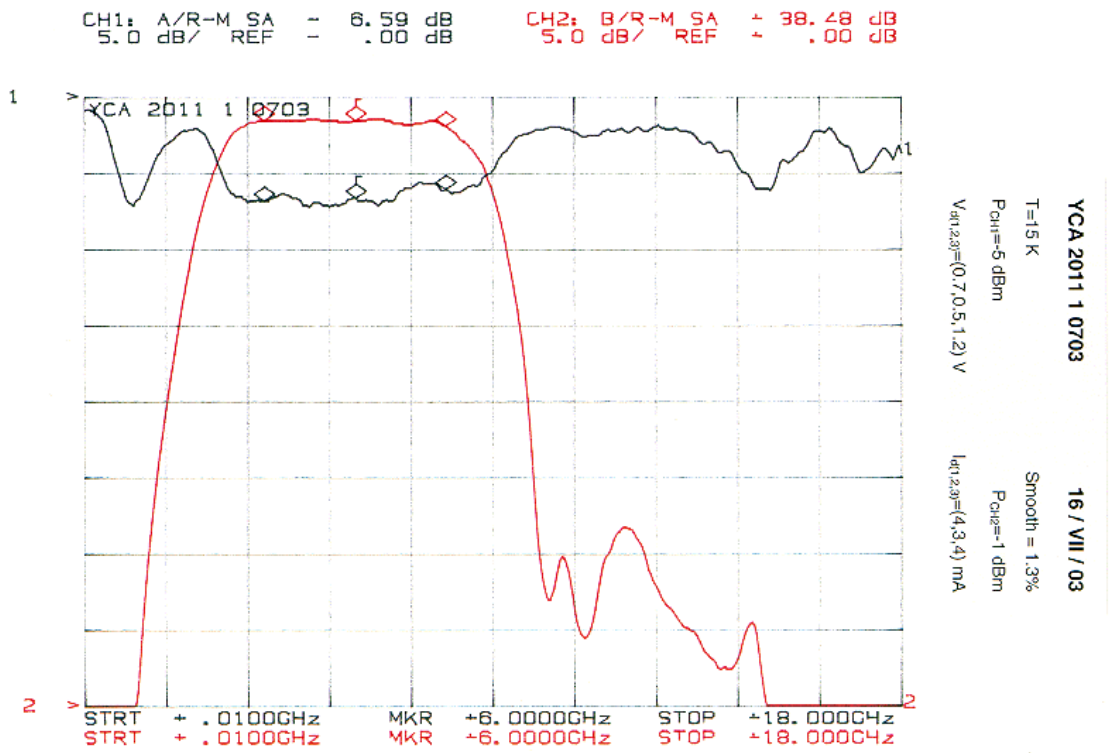
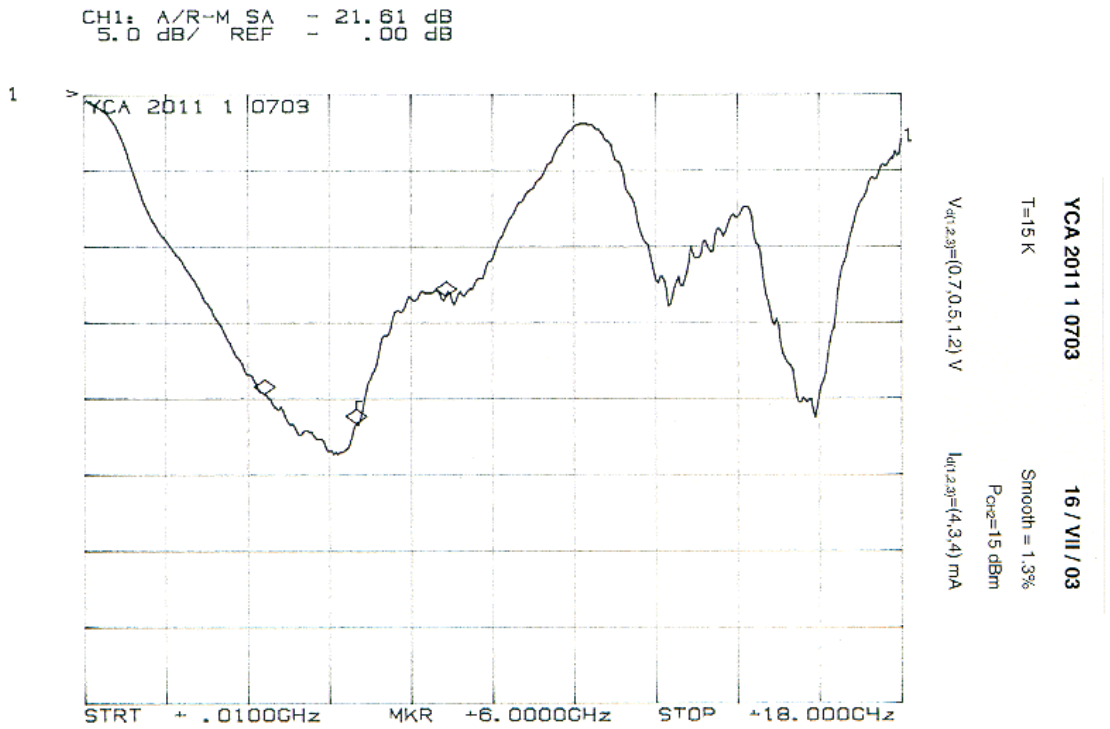
MODE: DSB (Freq>2.4 GHz)

YCA 2011 1 0703
(.7 4.05 1.36) (.5 2.98 .71) (1.21 4.05 .44) (0 .01 13.7) 15

Tmin= 3.58 K @ F= 4.600 GHz. Tmean= 3.83
GMIN= 38.55 dB GMAX= 39.55 dB
Tcold= 14.68 K NdB Table= 5

F	Gdut	Tdut	IF	RF	NdB	TH	TC
3.000	37.24	6.87	-25	-10	-2.28	195.0	23.4
3.200	38.03	6.07	-25	-10	-2.28	195.1	23.4
3.400	38.71	4.99	-25	-10	-2.27	195.3	23.4
3.600	38.96	4.32	-25	-10	-2.27	195.4	23.4
3.800	39.31	3.89	-25	-10	-2.26	195.5	23.4
4.000	39.33	3.60	-25	-10	-2.26	195.7	23.3
4.200	39.47	3.61	-25	-10	-2.25	196.1	23.3
4.400	39.55	3.60	-25	-10	-2.24	196.6	23.3
4.600	39.29	3.58	-25	-10	-2.22	197.1	23.3
4.800	39.35	3.58	-25	-10	-2.21	197.5	23.3
5.000	39.35	3.65	-25	-10	-2.20	198.0	23.2
5.200	39.37	3.87	-25	-10	-2.18	198.8	23.2
5.400	39.43	3.80	-25	-10	-2.16	199.6	23.2
5.600	39.35	3.91	-25	-10	-2.14	200.4	23.2
5.800	39.28	4.12	-25	-10	-2.12	201.1	23.2
6.000	39.32	3.78	-25	-10	-2.10	201.9	23.1
6.200	39.41	3.75	-30	-10	-2.07	203.0	23.1
6.400	39.26	3.77	-30	-10	-2.05	204.1	23.1
6.600	39.18	3.78	-30	-10	-2.02	205.1	23.1
6.800	39.07	3.96	-30	-10	-2.00	206.2	23.1
7.000	38.93	3.98	-30	-10	-1.97	207.3	23.0
7.200	39.10	4.00	-30	-10	-1.94	208.5	23.0
7.400	39.15	4.19	-30	-10	-1.91	209.8	23.0
7.600	39.16	3.95	-30	-10	-1.88	211.1	23.0
7.800	39.18	3.98	-30	-10	-1.85	212.4	23.0
8.000	38.55	4.05	-30	-10	-1.82	213.7	22.9
8.200	38.23	4.47	-30	-10	-1.79	215.1	22.9
8.400	37.60	4.73	-30	-10	-1.76	216.5	22.9
8.600	36.85	5.20	-30	-10	-1.72	217.9	22.9
8.800	36.13	6.21	-25	-10	-1.69	219.3	22.9
9.000	34.91	8.07	-25	-10	-1.66	220.7	22.8


CH1: A/R-M SA - 6.59 dB
5.0 dB/ REF - .00 dB
CH2: B/R-M SA + 38.28 dB
5.0 dB/ REF + .00 dB
YCA 2011 1 0703
STRT + .0100GHz MKR +6.0000GHz STOP +18.000GHz
STRT + .0100GHz MKR +6.0000GHz STOP +18.000GHz
YCA 2011 1 0703
16 / VII / 03
T=15 K
Smooth = 1.3%
P_CH1=-5 dBm
P_CH2=-1 dBm
V_d(1,2,3)=(0.7,0.5,1.2) V
I_d(1,2,3)=(4,3,4) mA


CH1: A/R-M SA - 21.61 dB
5.0 dB/ REF - .00 dB
YCA 2011 1 0703
STRT + .0100GHz MKR +6.0000GHz STOP +18.000GHz
YCA 2011 1 0703
16 / VII / 03
T=15 K
Smooth = 1.3%
P_CH2=15 dBm
V_d(1,2,3)=(0.7,0.5,1.2) V
I_d(1,2,3)=(4,3,4) mA

GAIN STABILITY TEST

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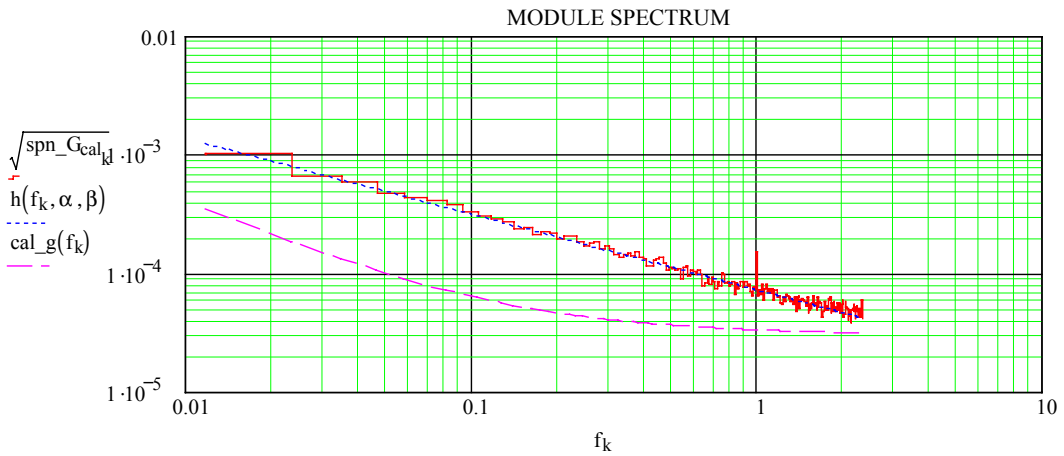
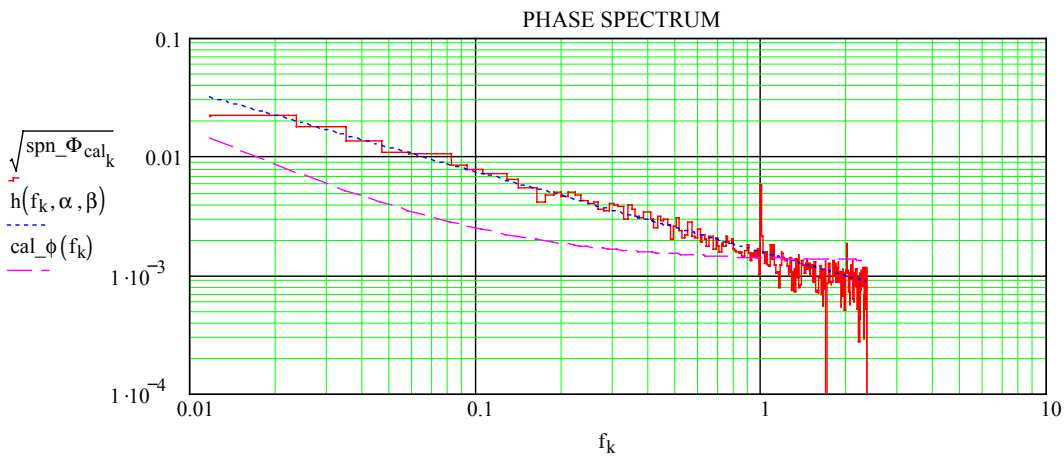
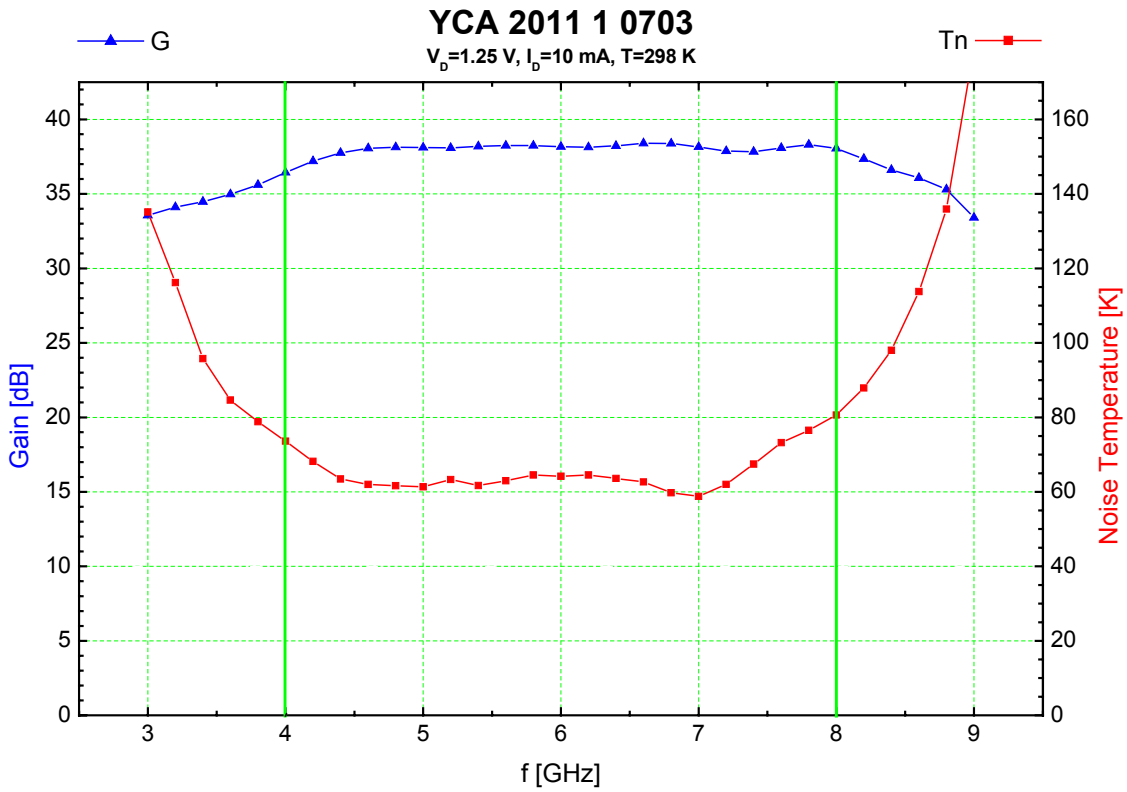


$\alpha = 0.678$ $\beta = 1.562 \times 10^{-3}$ $fit = \beta \cdot f^{-\alpha}$





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TIME 14:33:43 DATE : 14 Jul 2003 Tamb= 297.1

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YCA 2011 1 0703
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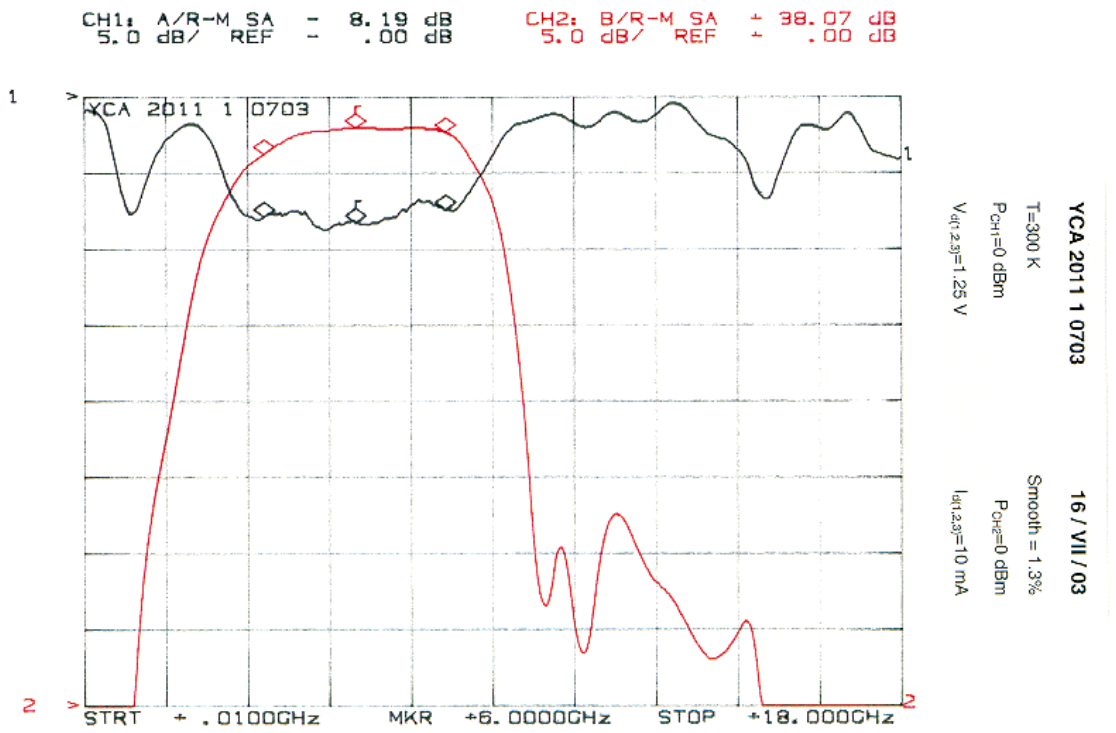
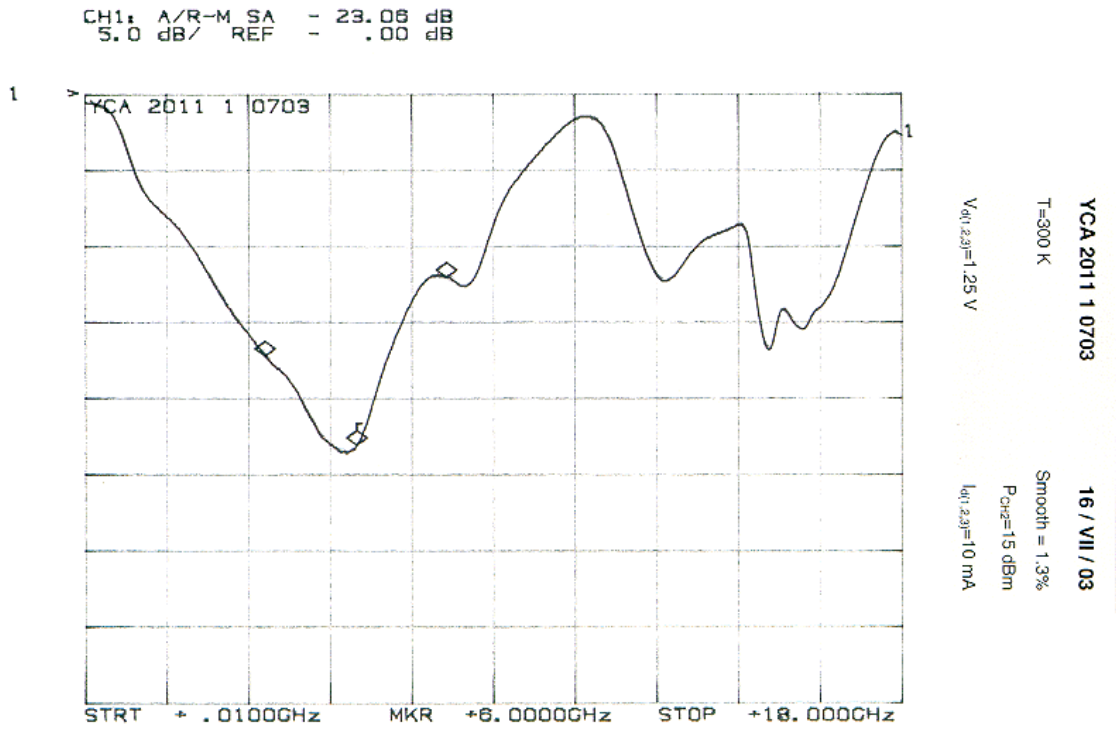
Tmin= 58.79 K @ F= 7.000 GHz. Tmean= 65.53
GMIN= 36.43 dB GMAX= 38.39 dB
Tcold= 300.00 K NdB Table= 1

F	Gdut	Tdut	IF	RF	NdB	TH	TC
3.000	33.56	135.10	-30	-10	+4.93	1192.4	300.0
3.200	34.11	116.19	-30	-10	+4.92	1191.2	300.0
3.400	34.47	95.77	-30	-10	+4.92	1189.9	300.0
3.600	34.97	84.64	-30	-10	+4.91	1188.7	300.0
3.800	35.61	78.80	-30	-10	+4.91	1187.4	300.0
4.000	36.43	73.62	-30	-10	+4.90	1186.2	300.0
4.200	37.19	68.16	-35	-10	+4.90	1186.2	300.0
4.400	37.75	63.46	-35	-10	+4.90	1186.2	300.0
4.600	38.06	61.99	-35	-10	+4.90	1186.2	300.0
4.800	38.13	61.65	-25	-20	+4.90	1186.2	300.0
5.000	38.11	61.33	-25	-20	+4.90	1186.2	300.0
5.200	38.08	63.31	-25	-20	+4.91	1188.7	300.0
5.400	38.19	61.69	-25	-20	+4.92	1191.2	300.0
5.600	38.24	62.98	-25	-20	+4.94	1193.6	300.0
5.800	38.24	64.52	-25	-20	+4.95	1196.1	300.0
6.000	38.16	64.18	-25	-20	+4.96	1198.7	300.0
6.200	38.13	64.54	-25	-20	+4.97	1199.9	300.0
6.400	38.22	63.60	-25	-20	+4.97	1201.2	300.0
6.600	38.39	62.66	-25	-20	+4.98	1202.4	300.0
6.800	38.38	59.78	-25	-20	+4.98	1203.7	300.0
7.000	38.15	58.79	-25	-20	+4.99	1205.0	300.0
7.200	37.87	62.02	-25	-20	+5.02	1210.9	300.0
7.400	37.83	67.46	-25	-20	+5.05	1216.8	300.0
7.600	38.08	73.21	-25	-20	+5.07	1222.8	300.0
7.800	38.30	76.53	-25	-20	+5.10	1228.9	300.0
8.000	38.05	80.63	-25	-20	+5.13	1234.9	300.0
8.200	37.35	87.88	-25	-20	+5.15	1239.3	300.0
8.400	36.61	98.01	-25	-20	+5.17	1243.7	300.0
8.600	36.07	113.77	-25	-20	+5.19	1248.1	300.0
8.800	35.30	135.91	-25	-20	+5.21	1252.5	300.0
9.000	33.40	179.18	-30	-10	+5.23	1256.9	300.0


CH1: A/R-M SA - 8.19 dB
5.0 dB/ REF - .00 dB
CH2: B/R-M SA + 38.07 dB
5.0 dB/ REF + .00 dB
YCA 2011 1 0703
STRT + .0100GHz
MKR +6.0000GHz
STOP +18.000GHz
YCA 2011 1 0703
T=300 K
Smooth = 1.3%
16 / VII / 03
P_{CH1}=0 dBm
P_{CH2}=0 dBm
$V_{d(1,2,3)}$=1.25 V
$I_{d(1,2,3)}$=10 mA


CH1: A/R-M SA - 23.06 dB
5.0 dB/ REF - .00 dB
YCA 2011 1 0703
STRT + .0100GHz
MKR +6.0000GHz
STOP +18.000GHz
YCA 2011 1 0703
T=300 K
Smooth = 1.3%
16 / VII / 03
P_{CH2}=15 dBm
$V_{d(1,2,3)}$=1.25 V
$I_{d(1,2,3)}$=10 mA

GAIN STABILITY TEST

cal_file:= "cal_data\cal.prn"

$N_{scans} := 50$

data_directory:= "YCA_2011_AMB"

file_preffix= "F" file_suffix= ".prn"

out_file:= "results.prn"

Frequency range for the fit: $f_fit_{min} := 0.1$ $f_fit_{max} := 0.9$

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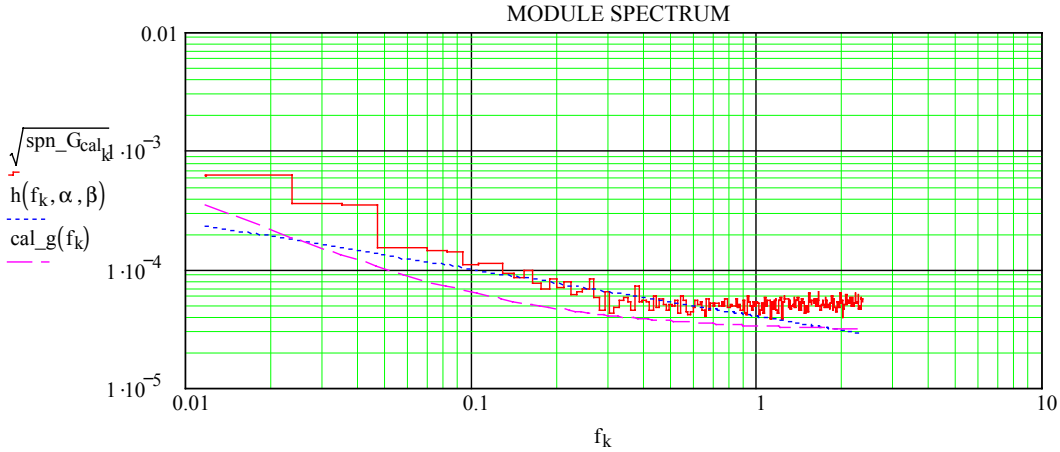
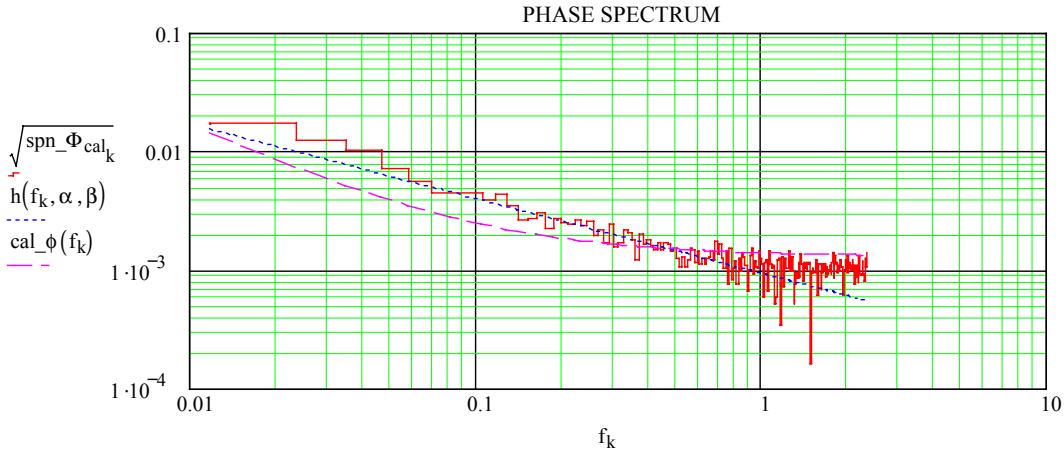
$\alpha = 0.396$ $\beta = 4.006 \times 10^{-5}$ $fit = \beta \cdot f^{-\alpha}$



$\alpha = 0.628$ $\beta = 9.404 \times 10^{-4}$ $fit = \beta \cdot f^{-\alpha}$



HEMT BIAS CARD REPORT

1. Introduction

A power supply card is needed to operate the amplifier. This report provides information about an NRAO-style design for a power supply card manufactured at CAY. The schematic is presented in figure 1. Drawings of the PC board and details of the connectors are presented in the included documentation.

2. Description and operation

The power supply card provides signals to monitor the correct operation of each of the stages of the amplifiers, and to facilitate the adjustment. The parameters available are the drain voltage (V_d), drain current (I_d) and gate voltage (V_g). Note that the monitor signal of the drain current provides a voltage reading proportional to the current (0.1 V per mA, for Id=5 mA the reading is 0.5 Volt). The monitor signals are available in the PCB edge connector pins, and as test points in the front part of the PCB.

The power supply is a feedback system implemented with a quad operational amplifier per each HEMT amplifier stage, and can be easily understood observing the attached schematic for a single stage (figure 1). The desired drain voltage and drain current of the HEMT are selected in variable resistors, and the power supply finds the adequate value of the gate voltage. In these way, any change in the transconductance of the HEMT is compensated by changing the gate voltage, keeping the drain current constant.

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Addendum: Modifications to the standard design

To allow a sufficient range of gate voltages when using amplifiers with gate voltage dividers, zenner diodes D3, D6, D9 and D12 have been replaced by two zenner diodes of the same type connected in opposition (anti-series).

Important: This changes affect figures 1,2,5 and table 1

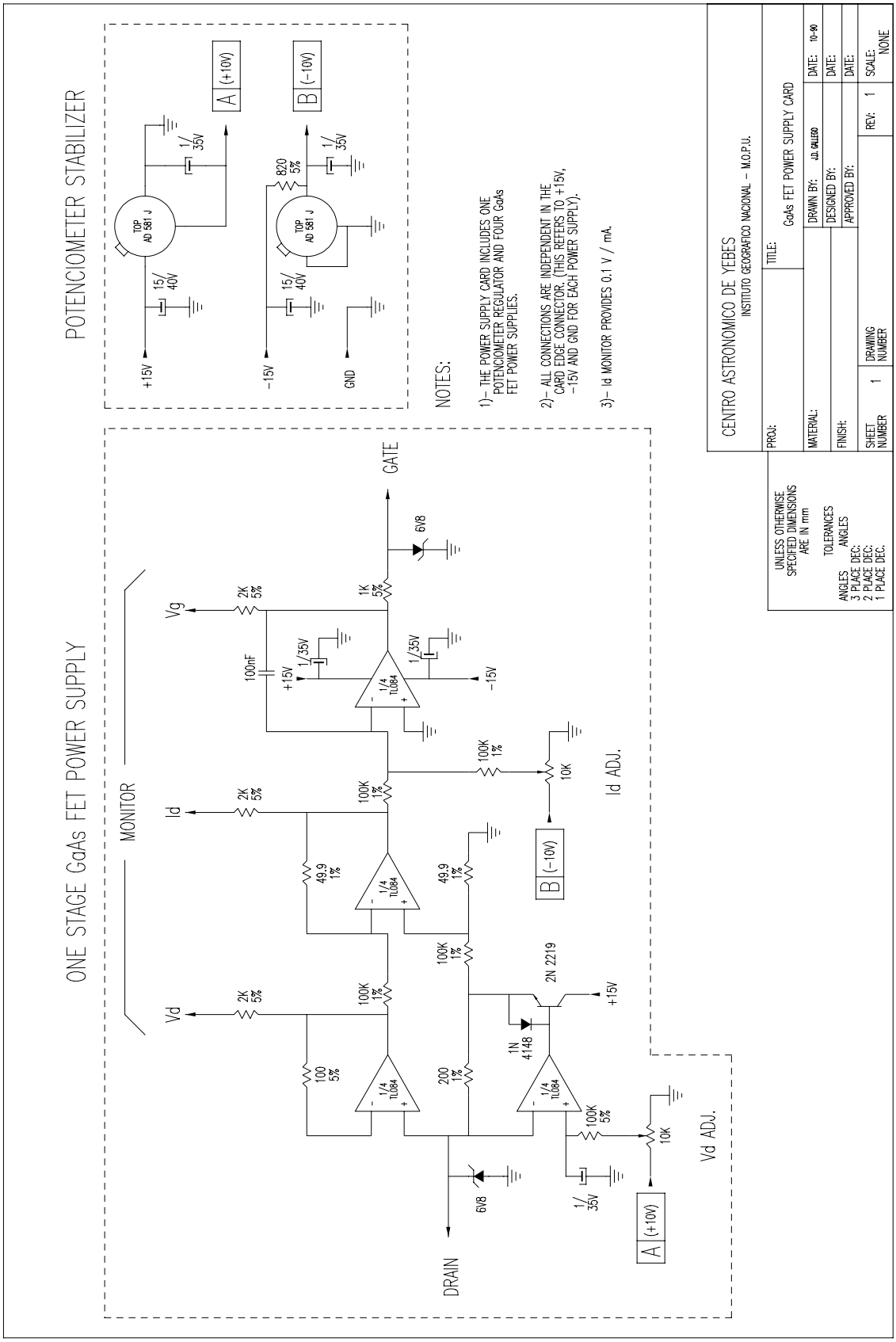

Figure 1: *One stage schematic*

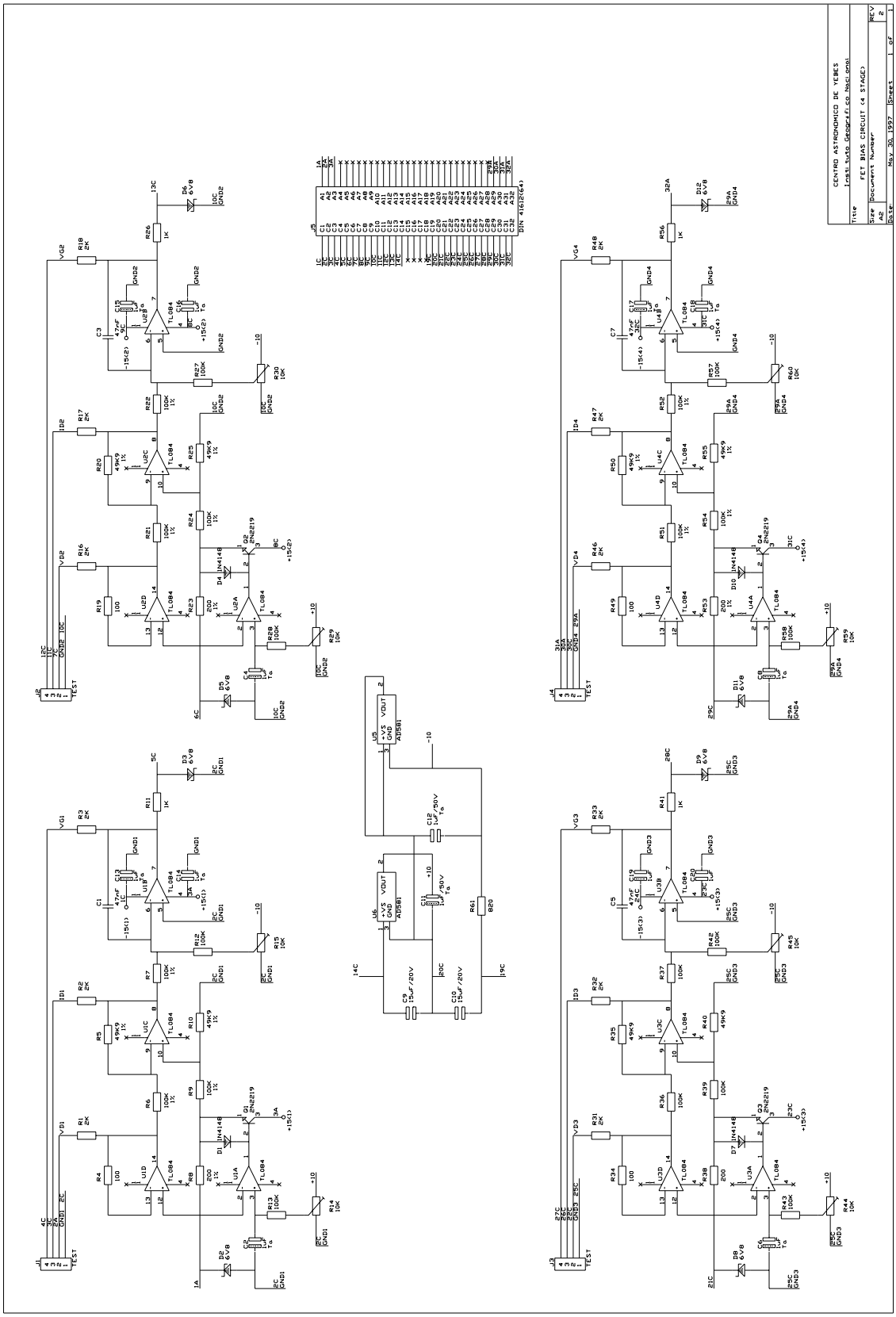

Figure 2: *PC Board schematic*

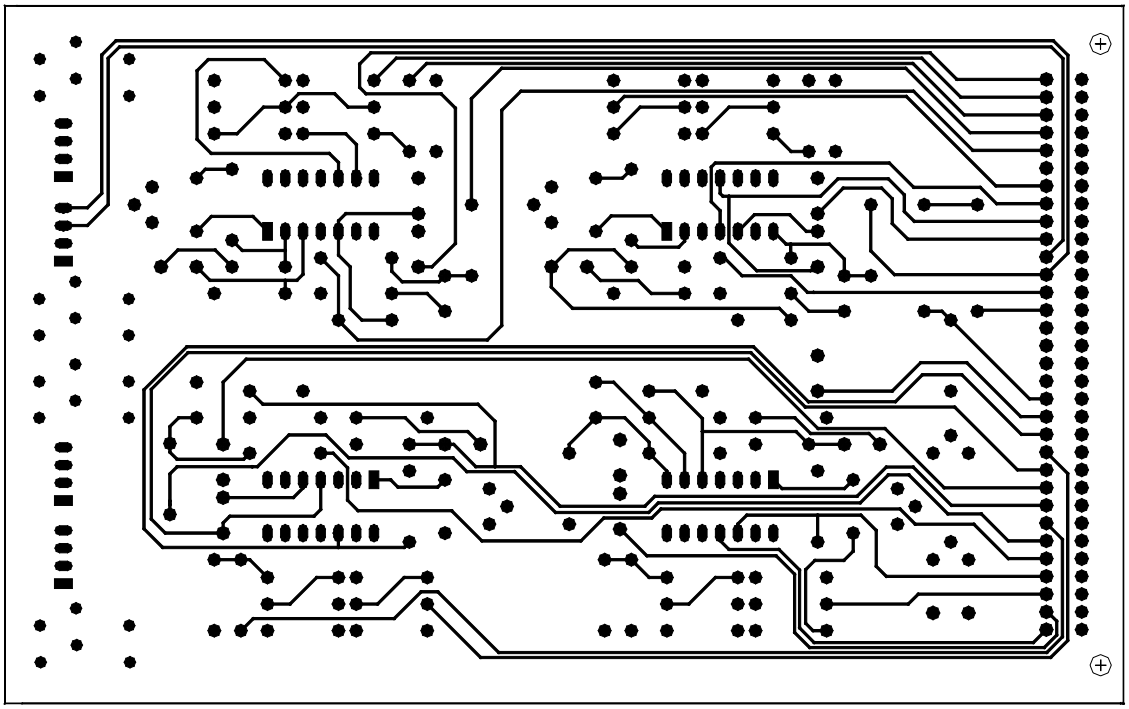

Figure 3: *PC Board tracks - Component side*

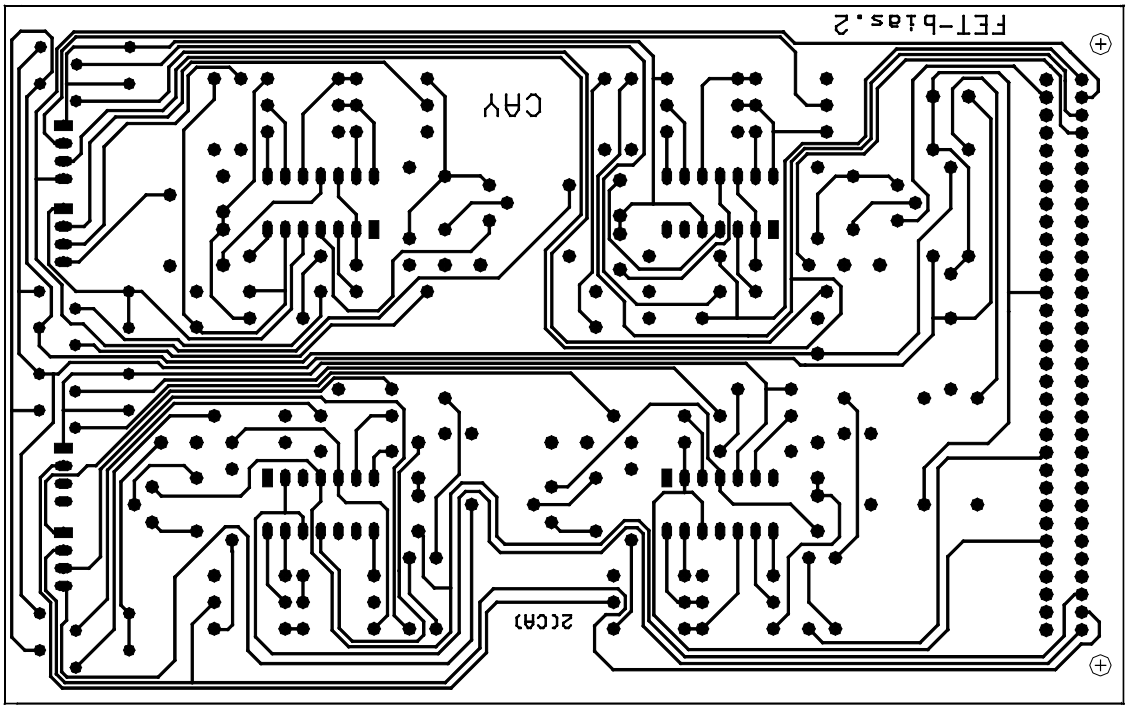

Figure 4: *PC Board tracks – Solder side*

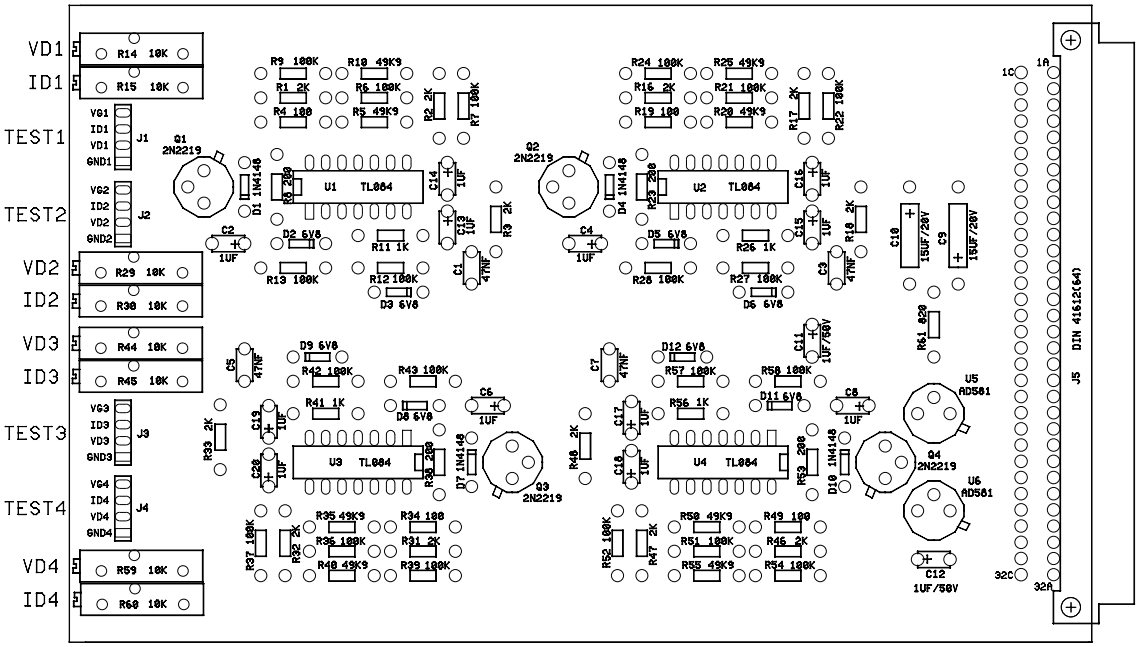

Figure 5: *PC Board components*

Table 1: *Power supply list of components*

FET BIAS CIRCUIT (4 STAGE) Revised: January 31, 1997
Revision: 2

Bill Of Materials March 20, 1997 Page 1

Item	Quantity	Reference	Part	DESCRIPTION
1	4	C1,C3,C5,C7	47nF	Polyester, 63V
2	12	C2,C4,C6,C8,C11,C12,C13, C14,C15,C16,C17,C18,C19, C20	1uF	Tantalum, 50V
3	2	C10,C9	15uF/20V	Electrolytic
4	8	D2,D3,D5,D6,D8,D9,D11, D12	6V8	
5	4	D1,D4,D7,D10	1N4148	
6	4	J1,J2,J3,J4	TEST	4pin, SIL BAR
7	1	J5	DIN 41612(64)	
8	4	Q1,Q2,Q3,Q4	2N2219	
9	12	R1,R2,R3,R16,R17,R18,R31, R32,R33,R46,R47,R48	2K	1/4W, 1%
10	4	R4,R19,R34,R49	100	1/4W, 5%
11	8	R5,R10,R20,R25,R35,R40, R50,R55	49K9	1/4W, 1%
12	20	R6,R7,R9,R12,R13,R21,R22, R24,R27,R28,R36,R37,R39, R42,R43,R51,R52,R54,R57, R58	100K	1/4W, 1%
13	4	R8,R23,R38,R53	200	1/4w, 1%
14	4	R11,R26,R41,R56	1K	1/4W, 5%
15	8	R14,R15,R29,R30,R44,R45, R59,R60	10K	20T H POT
16	1	R61	820	1/4W, 5%
17	4	U1,U2,U3,U4	TL084	
18	2	U6,U5	AD581	

Table 2: *PC Board edge connector wiring table*

DIN 41612

PIN NUMBER	DESCRIPTION	PIN NUMBER	DESCRIPTION
1 a	DRAIN 1 (1)	11 c	Id (2)
2 a	Vd 1 (1)	12 c	Vg (2)
3 a	+15 V (1)	13 c	GATE (2)
-	-	14 c	+15 V (to potenc.)
29 a	GND (4)	-	-
30 a	Id (4)	19 c	-15 V (to potenc.)
31 a	Vg (4)	20 c	GND (to potenc.)
32 a	GATE (4)	21 c	DRAIN 3
-	-	22 c	Vd (3)
1 c	-15 V (1)	23 c	+15 V (3)
2 c	GND (1)	24 c	-15 V (3)
3 c	Id (1)	25 c	GND (3)
4 c	Vg (1)	26 c	Id (3)
5 c	GATE (1)	27 c	Vg (3)
6 c	DRAIN (2)	28 c	GATE (3)
7 c	Vd (2)	29 c	DRAIN (4)
8 c	+15 V (2)	30 c	Vd (4)
9 c	-15 V (2)	31 c	+15 V (4)
9 c	-15 V (2)	32 c	-15 V (4)
10 c	GND (2)		

Table 3: *Cable connections for a 3-stage HEMT amplifier*

15 PIN 'D' CONNECTOR (BIAS MONITOR)

PIN NUMBER	DESCRIPTION
1	SIGNAL GROUND
2	Vd 1
3	Id 1
4	Vg 1
5	Vd 2
6	Id 2
7	Vg 2
8	Vd 3
9	Id 3
10	Vg 3
11	N.C.
12	N.C.
13	N.C.
14	N.C.
15	N.C.

9 PIN 'D' CONNECTOR (TO HEMT AMPLIFIER)

PIN NUMBER	DESCRIPTION
1	SIGNAL GROUND
2	DRAIN 1
3	GATE 1
4	DRAIN 2
5	GATE 2
6	DRAIN 3
7	GATE 3
8	N.C.
9	N.C.

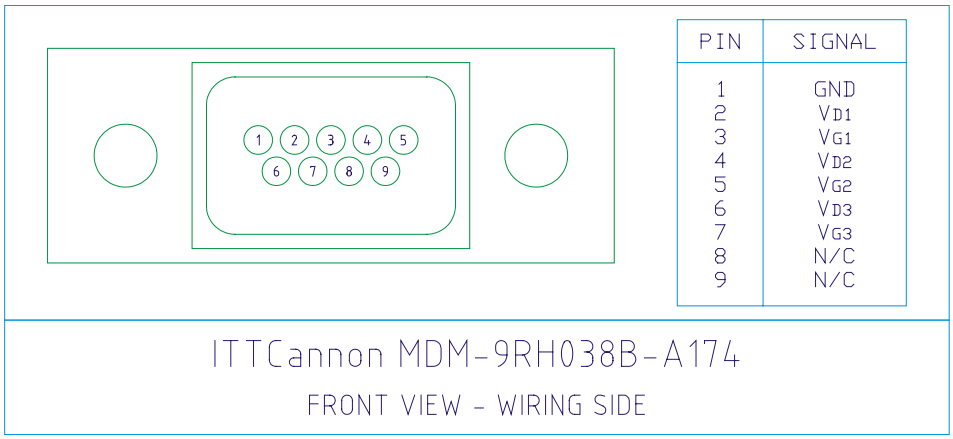

Figure 6: *Microtech connector plug (in cable) for a 3-stage HEMT amplifier*

ESD AND POWER SUPPLY LEAKAGE PROTECTION OF InP CRYOGENIC HEMT AMPLIFIERS

Introduction

Cryogenic amplifiers made with InP HEMTs have been found very sensitive to ESD (electrostatic discharges) and leakage from the power supplies. The handling of these devices requires especial precautions beyond the normal care taken with cryogenic amplifiers made with commercial GaAs HEMTs. Especial procedures should be followed during assembly of the amplifiers as well as during tests and operation to avoid permanent damage to the devices. The most common mode of failure is the total or partial destruction of the gate of the transistors. Partially damaged devices may loose one or more gate fingers and show poor or no pinch off, even if the gate junction still show diode characteristics. Totally damaged devices may appear as a short circuit (or low resistance) from drain to source. Sometimes, but not often, the device may appear as an open circuit.

ESD is not the only problem. Leakage of soldering irons, bonding machines and even power supplies of the amplifiers has produced many failures. All the equipment used in the assembly test and operation of the amplifiers should be checked for leakage. Most of the field problems detected have been caused by 50 Hz current leakage of input transformers of floating DC power supplies. This leakage is due to the capacitive coupling between primary and secondary of the transformers and it is always present unless there is a grounded faraday shield between the two windings or other especial precautions are taken

Procedure for assembly of the amplifiers

1. Technicians manipulating amplifiers should wear grounded wrist straps.
2. The bench for the assembly of the amplifiers should have a dissipative map connected to ground.
3. A short circuit should be put in the power connector of the amplifier at all times during assembly (the short circuit should short all pins together to the case). The short circuit will only be removed for testing the amplifier or when connected for operation.
4. Coaxial SMA short circuits should be connected to input and output RF connectors at all times during assembly. The short circuits will only be removed for testing the amplifier or when connected for operation.
5. The soldering irons used for assembly should be adequately grounded. It should be checked that no voltage respect to ground is measured on the tip with the soldering iron on and off. The maximum voltage allowed will be 0.020 Vrms respect to ground measured with a high input impedance (> 10 MΩ) voltmeter in AC mode.
6. The tip of the bonding and welding machines used for assembly of the amplifier should be adequately grounded. It should be checked that no voltage respect to ground is measured with machines on or off. The maximum voltage allowed will be 0.020 Vrms respect to ground measured with a high input impedance (> 10 MΩ) voltmeter in AC mode.

7. Be very careful with any measurement instrument used during assembly. If ohmmeters are used for verification of internal cabling, battery operated units are preferred. Make all necessary verifications before the assembly of the transistors when possible. The assembly of the transistors should be the last operation to avoid unnecessary risks.

Procedure for test and operation of the amplifiers

1. The amplifier should be kept with a short circuit in the power connector when not in use. The short circuit should short all pins together and to the case. The short circuit should only be removed if adequate ESD and leakage protection precautions have been taken.
2. Most failures in cryogenic amplifiers are produced when connecting or disconnecting the amplifier to/from the power supply. **A very careful procedure should be followed**.
3. Make sure that the power supply is **off** before connecting or disconnecting the power supply cable to/from the amplifier.
4. Make sure that the power supply and the amplifier are connected to the same protective ground before connecting or disconnecting the power supply cable to/from the amplifier.
5. Very especial care should be taken in case of a DC power supply floating respect to the protective ground. This produces most failures. It is safer to connect the **return** terminal at the output of the DC power supply to the protective **ground** permanently on the power supply side. If this is not possible (for example to avoid ground loops with long cables), a provisional connection from the return of the power supply to the amplifier case should be **made prior to any connection or disconnection** of the power supply cable. Always make sure that there is no voltage between the return of the power supply and the protective ground (case of the amplifier) before connecting the power supply cable. The maximum allowed voltage will be 0.020 Vrms measured with a high input impedance (> 10 MΩ) voltmeter in AC mode.
6. The power supply should have adequate built in protection to avoid excessive voltage and currents in the transistors in case of power supply failure and during the transients produced when the power supply is switched on or off. Adequate Zenner diodes can be used in parallel with the outputs, and adequate series resistors in series. If the protections are designed adequately, the amplifier will survive even in case of errors in the connections of the cables.

Storage of the amplifiers

1. The amplifiers should be stored in a clean dry anti-static environment.
2. The amplifier should be stored with short circuits in the power and RF connectors.
3. For permanent storage desiccators with less than 20% relative humidity should be used. The preferred method of storage is in dry nitrogen containers.
4. For transportation, and for short-term storage, anti-static plastic bags with silica gel bags to keep low relative humidity should be used.